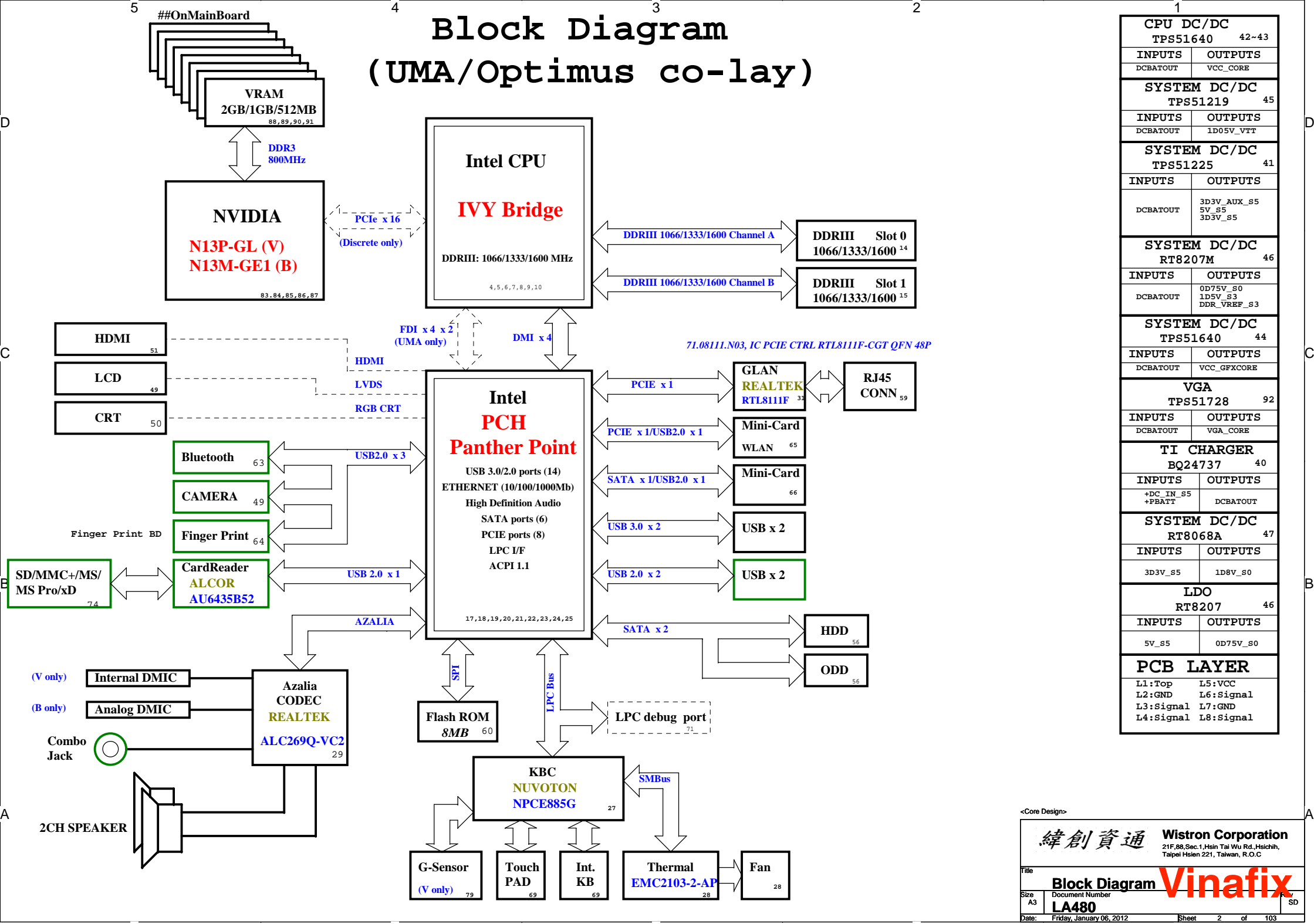


Block Diagram (UMA/Optimus co-lay)



PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV
Device		Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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Title

Table of Content

Size A3

Document Number

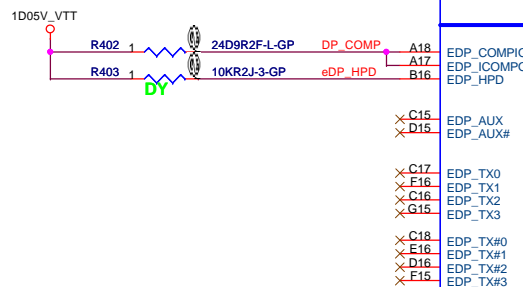
Rev SD

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01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

Signal Routing Guideline:
PEG ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG ICOMPI & PEG RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

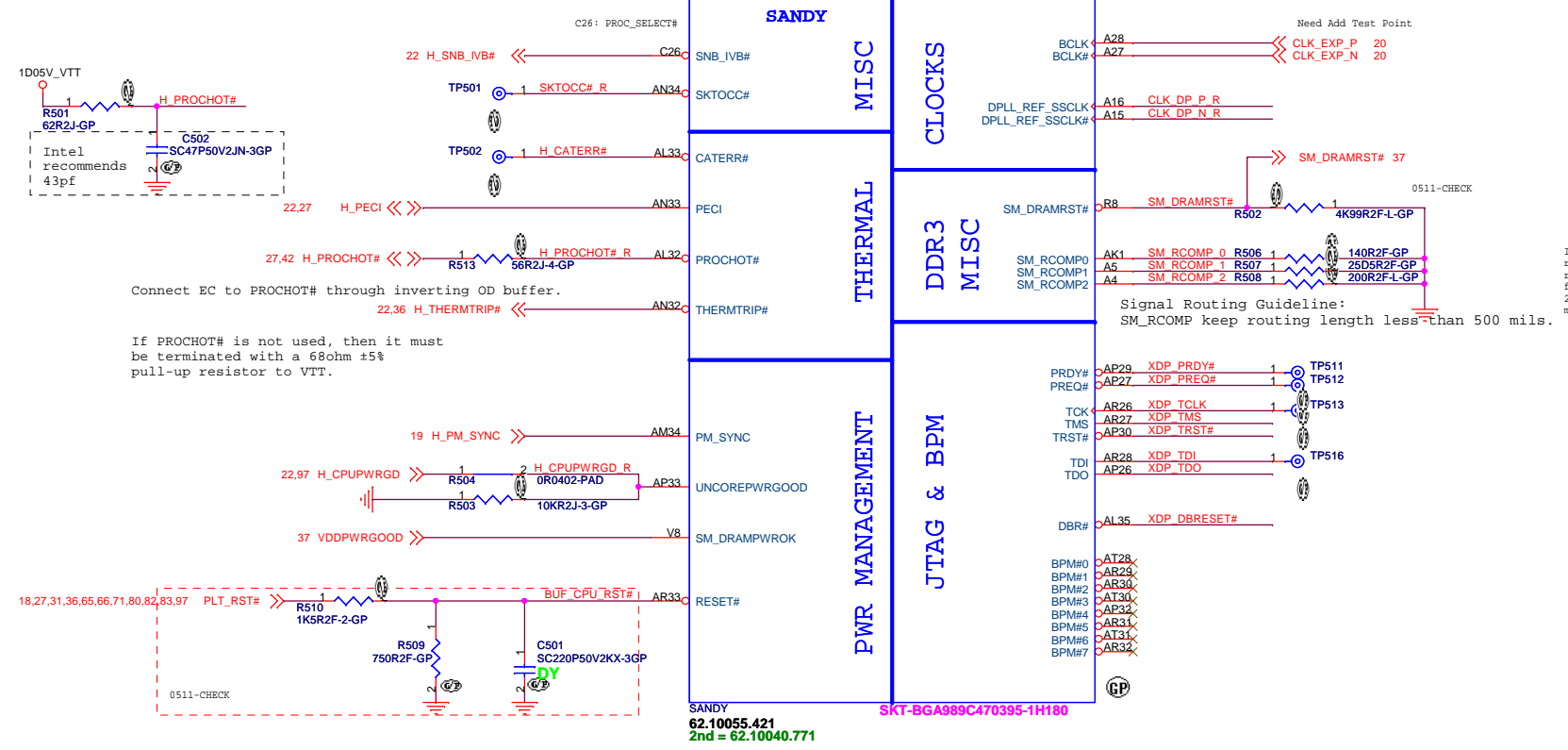


NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

Title			
CPU (PCIE/DMI/FDI)			
Size A3	Document Number LA480	Rev SD	
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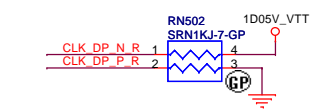
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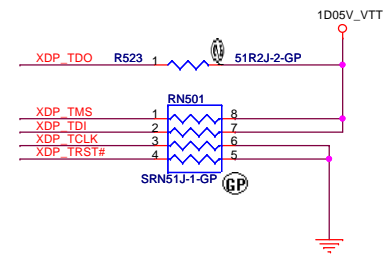
DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

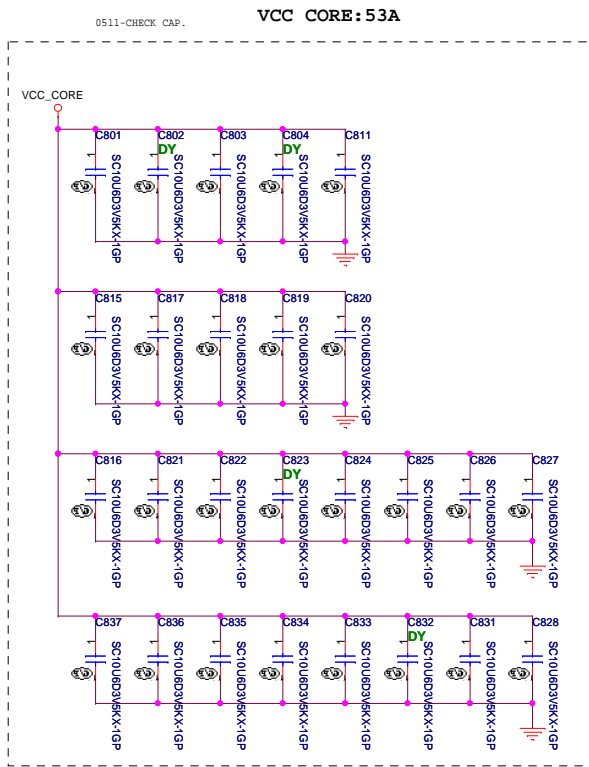
ASM R510
ASM R509

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.



In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.





VCC_CORE

CPU1F

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
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AA28 VCC
AA27 VCC
AA26 VCC
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Y30 VCC
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Y28 VCC
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Y26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
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Y29 VCC
Y28 VCC
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U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

SANDY

POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT#
VIDCLK
VIDSOUT

VCC_SENSE
VSS_SENSE

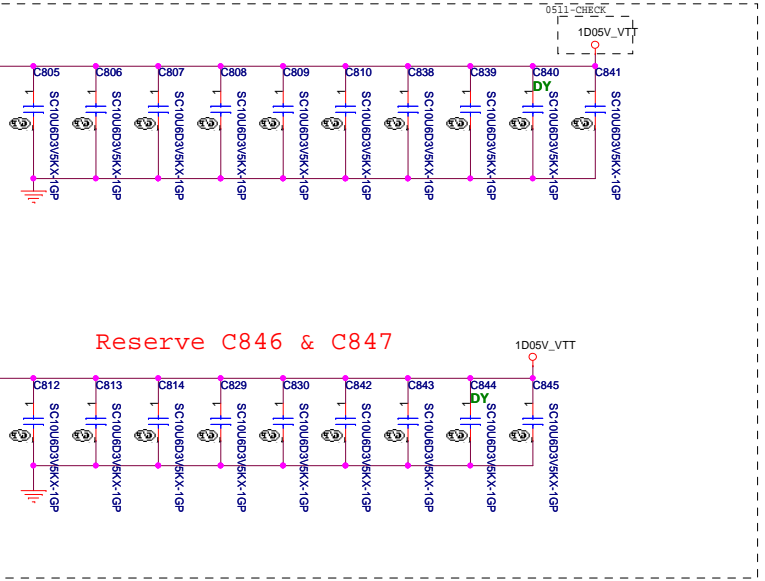
VCCIO_SENSE
VSSIO_SENSE

VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO L10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12
VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
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VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

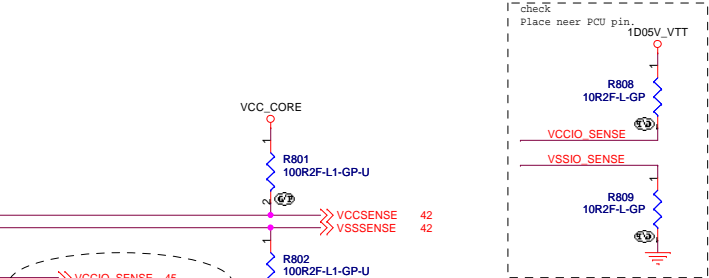
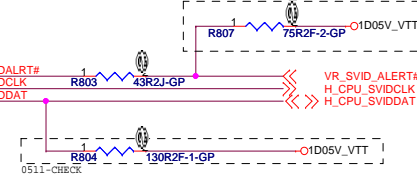
6 OF 9

0511-CHECK CAP.

VCCIO:8.5A



For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

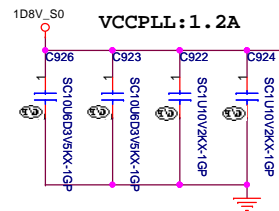


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Custom	LA480			
Date:	Friday, January 06, 2012	Sheet	8	of 103

SANDY
62.10055.421
2nd = 62.10040.771



SANDY

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

SANDY
62.10055.421
2nd = 62.10040.771

7 OF 9

SM VREF

VDDQ: 5A

VCCA: 6A

```
+V0.85S - VCCSA - System Agent rail voltage can be
[0.9, 0.725, 0.8, 0.675] V for IVB
[0.9, 0.8] V for SNB
```

VAXG_SENSE
VSSAXG_SENSE

```

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

```

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V SM VREF CNT should have 10 mil trace width

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

VDDQ	AF7
VDDQ	AF4
VDDQ	AF1
VDDQ	AC7
VDDQ	AC4
VDDQ	AC1
VDDQ	Y7
VDDQ	Y4
VDDQ	Y1
VDDQ	U7
VDDQ	U4
VDDQ	U1
VDDQ	P7
VDDQ	P4
VDDQ	P1

VCCSA	M27
VCCSA	M26
VCCSA	L26
VCCSA	J26
VCCSA	J25
VCCSA	J24
VCCSA	H26
VCCSA	H25

VCCSA SENSE

FC_C22
VCCSA_VID1RN901
SRN1KJ-7-GP

VCC_GFXCORE

VCC_AXG_SENSE
VSS_AXG_SENSE

1.1.05.11

1-1-GP-U

<Core Design>

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Title

CPU (VCC_GFXCORE)

Size

Document Number

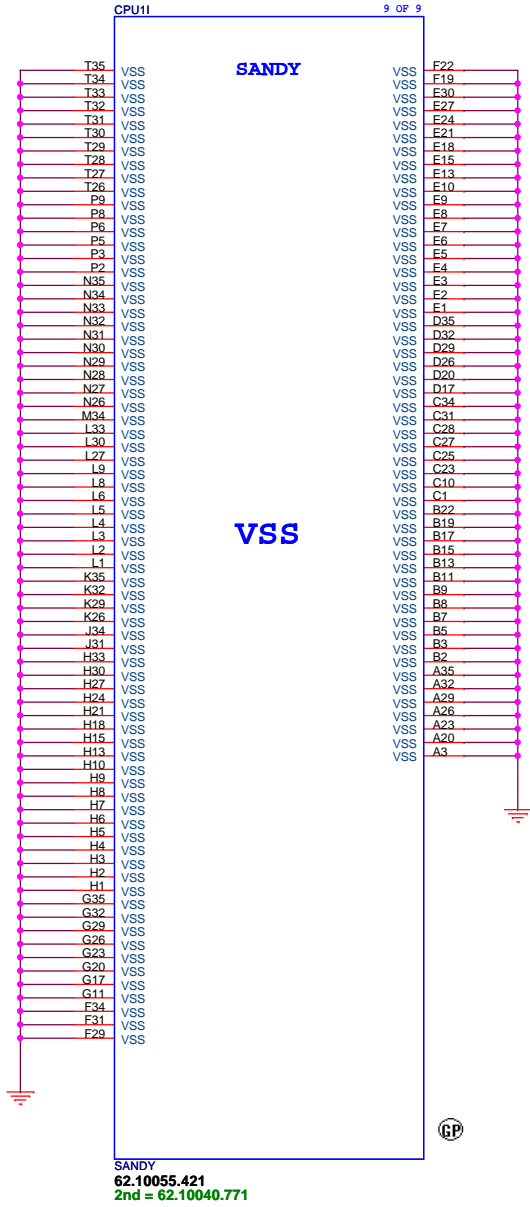
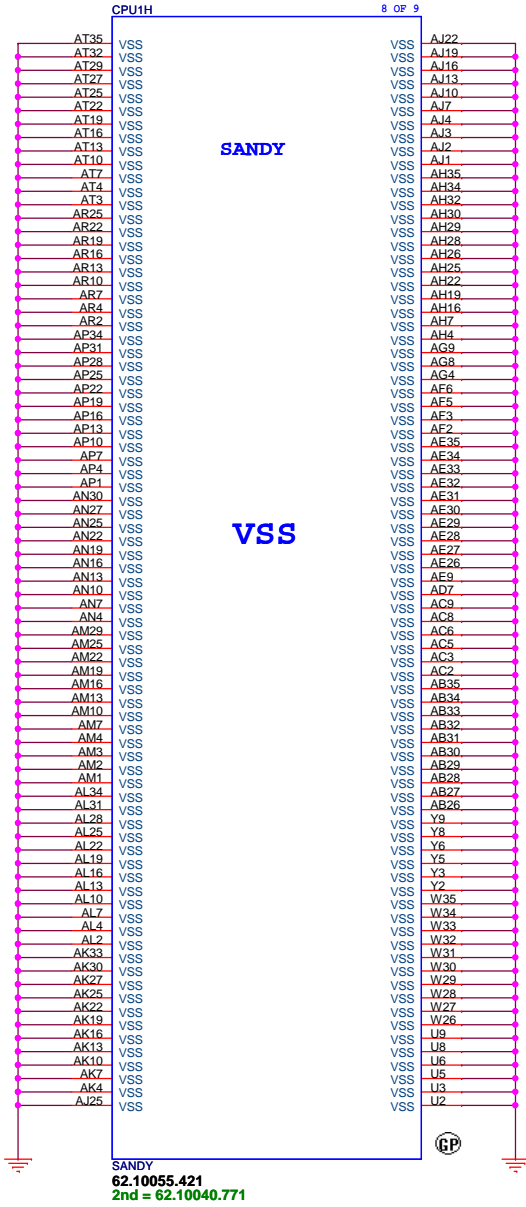
Rev

LA480

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SSID = CPU



D

C

B

A

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Title <Title>		
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CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



D

C

B

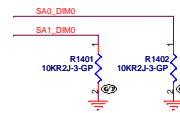
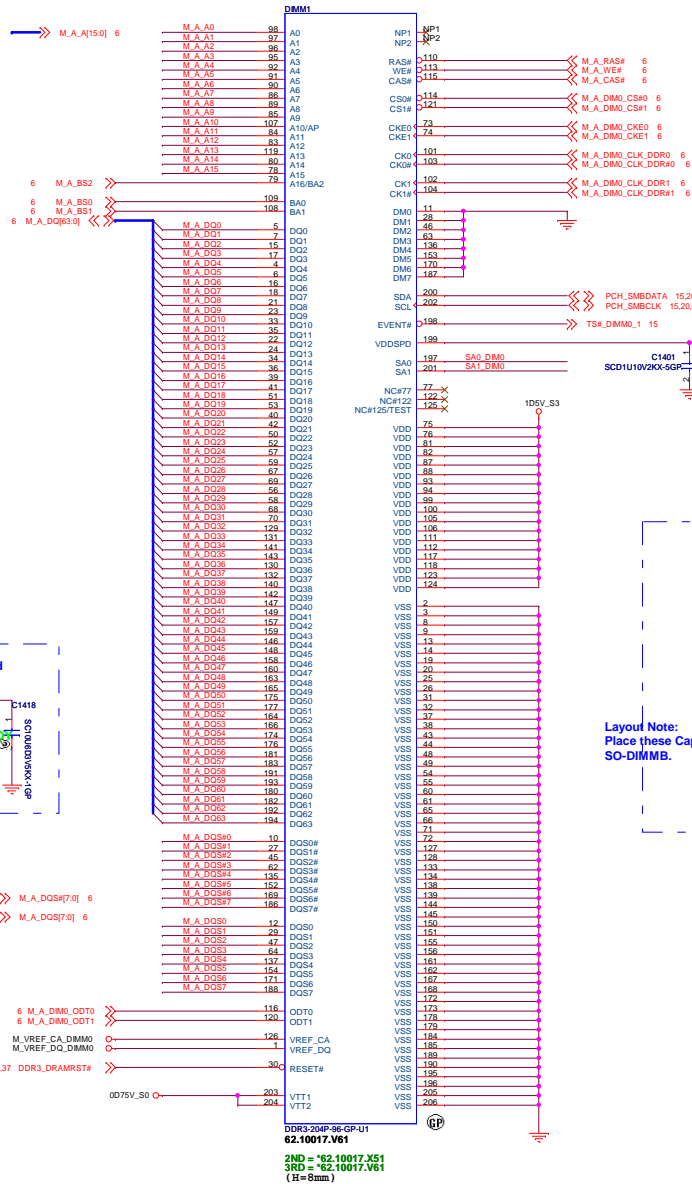
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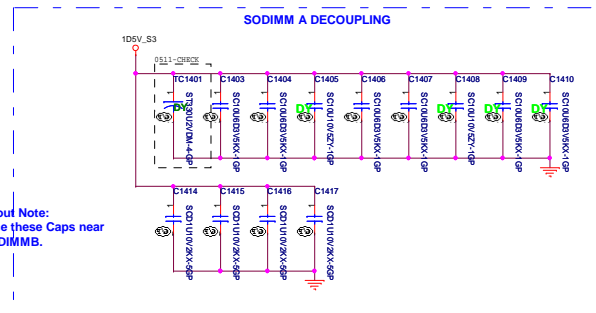
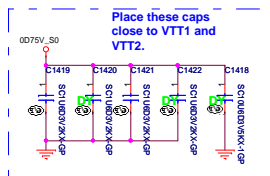
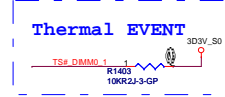
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SSID = MEMORY

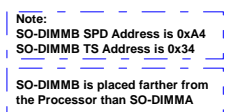


Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA
SO-DIMMA TS Address is 0x30

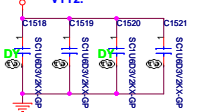
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near
SO-DIMMB.

[illegible]

Place these caps close to VTT1 and VTT2



```
>> M_B_DQS#(7:0)
>> M_B_DQS(7:0) 6
```

6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1
M_VREF_CA_DIMM1
M_VREF_DQ_DIMM1
DDR3_DRAMRST#

0D75V_S0 

(H=4mm)

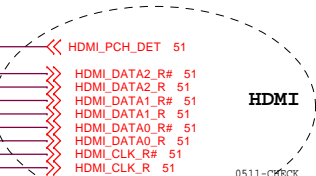
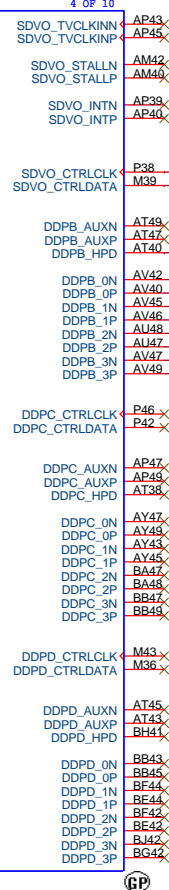
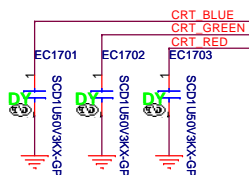
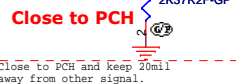
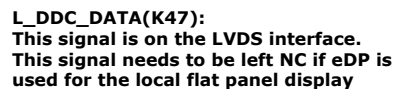
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3rd = *62.10017.V51

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3RD:62.10017.V51

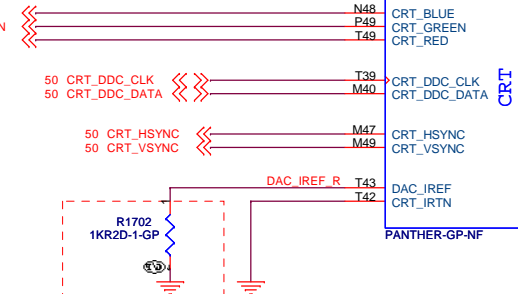
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Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>LA480</div>	Rev <div>SD</div>
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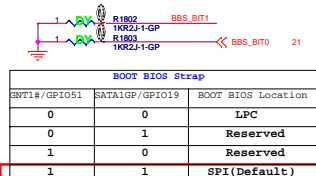
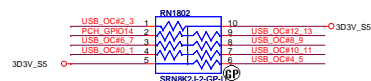
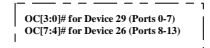
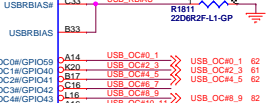
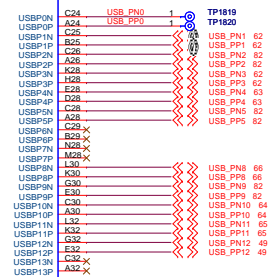
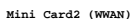
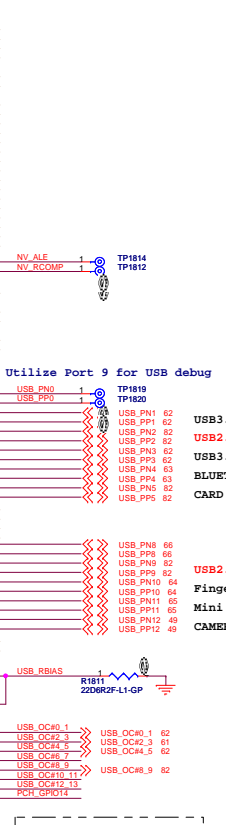
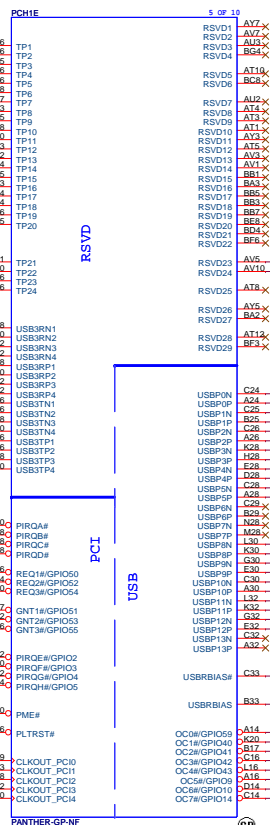
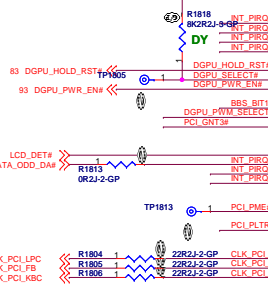
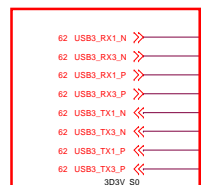
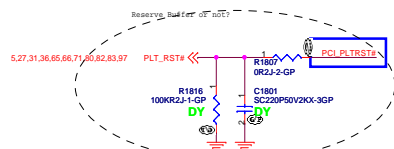
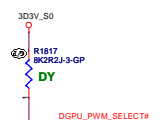
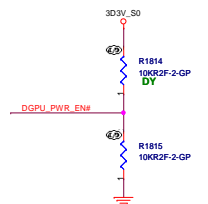
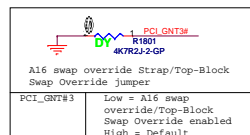
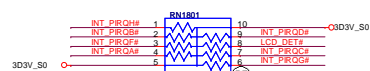
PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	TMDSB_CLK#
	DDPB_RX1P	NA
	DDPB_RX1N	NA
	DDPB_RX2P	HDMI1_HPD
	DDPB_RX2N	HDMI1_CTRLCLK
	SDVO_CTRLCLK	HDMI1_CTRLCLK
	SDVO_CTRLDATA	HDMI1_CTRLDATA



Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k $\pm 0.5\%$. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

SSID = PCH



BOOT BIOS Strap		
ENT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

For platforms not supporting Deep S4/S5
1.VccDSW3.3 and VccDSW3.3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARR# used as SUSPWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

Platforms supporting Deep S4/S5:
1.VccDSW3.3 and VccDSW3.3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARR# used as SUSPWRDNACK/GPIO30

SUSACK# : For non-DW platforms, this signal can be left unconnected.
Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed.

SYS_PWROK : the system is ready to start the exit from reset (de-asserts P2C_S0P# to the processor)
PWROK : it indicates to PCH that its CORE well power is stable.

Active Sleep Well (ASW) Power OK
S0_PWR_GOOD after PM_SLP_S3H delay 200 ms

SUSPWRDNACK : No longer requires a 10-K pull-up to VccDSW (3.3 V).

PCH_WAKE#
CRB : 1K
CHKLIST : 10K

This signal is used to control power planes to the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timing as SLP_S3#.

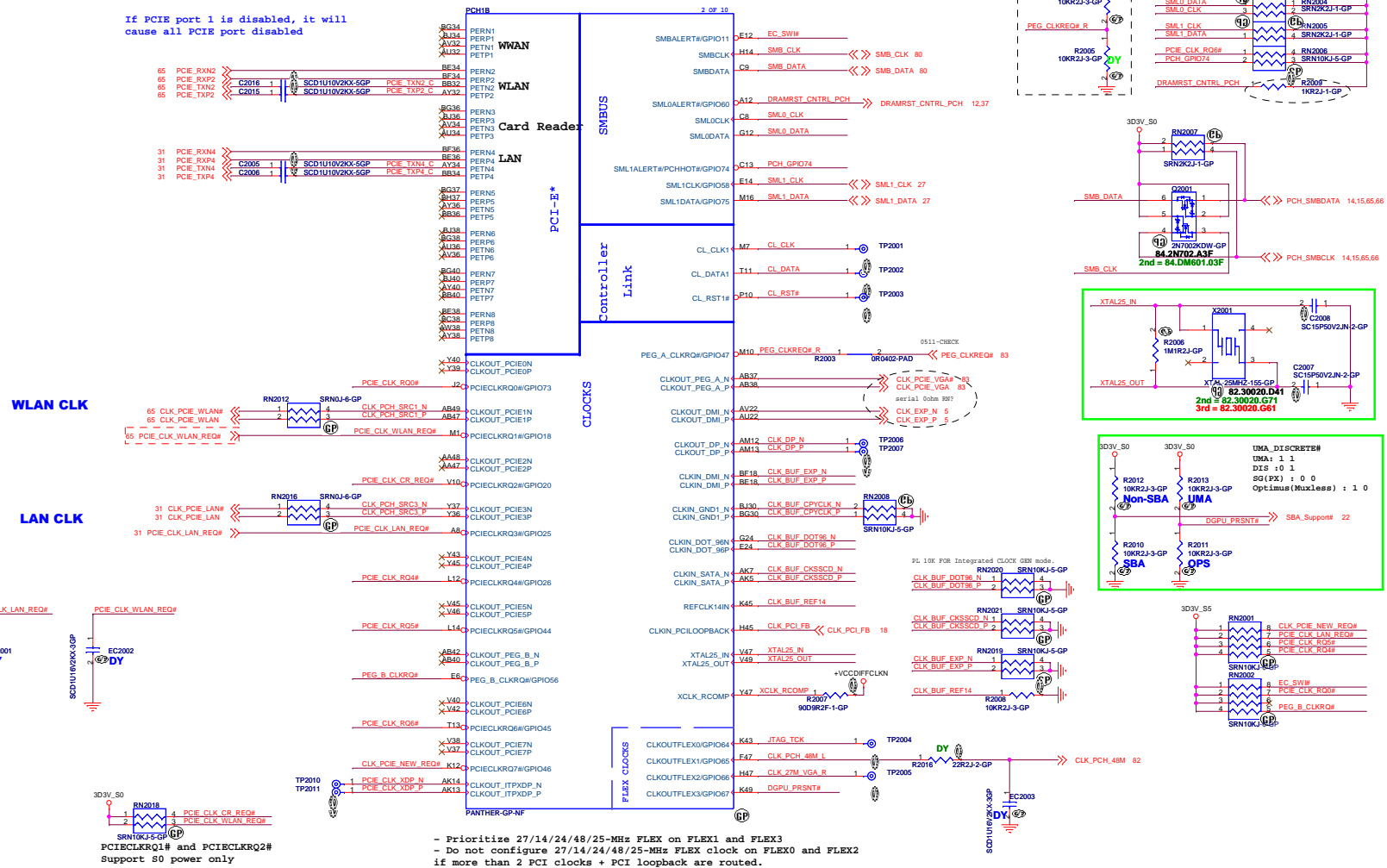
For platforms supporting Deep S4/S5 state, a low on this signal indicates that PCH is in Deep Sleep state and that EC/platform logic does not need to keep the Suspend Rails ON.
If high means EC must keep SUS rails ON.
If Deep S4/S5 is not supported, then this pin can be left unconnected.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

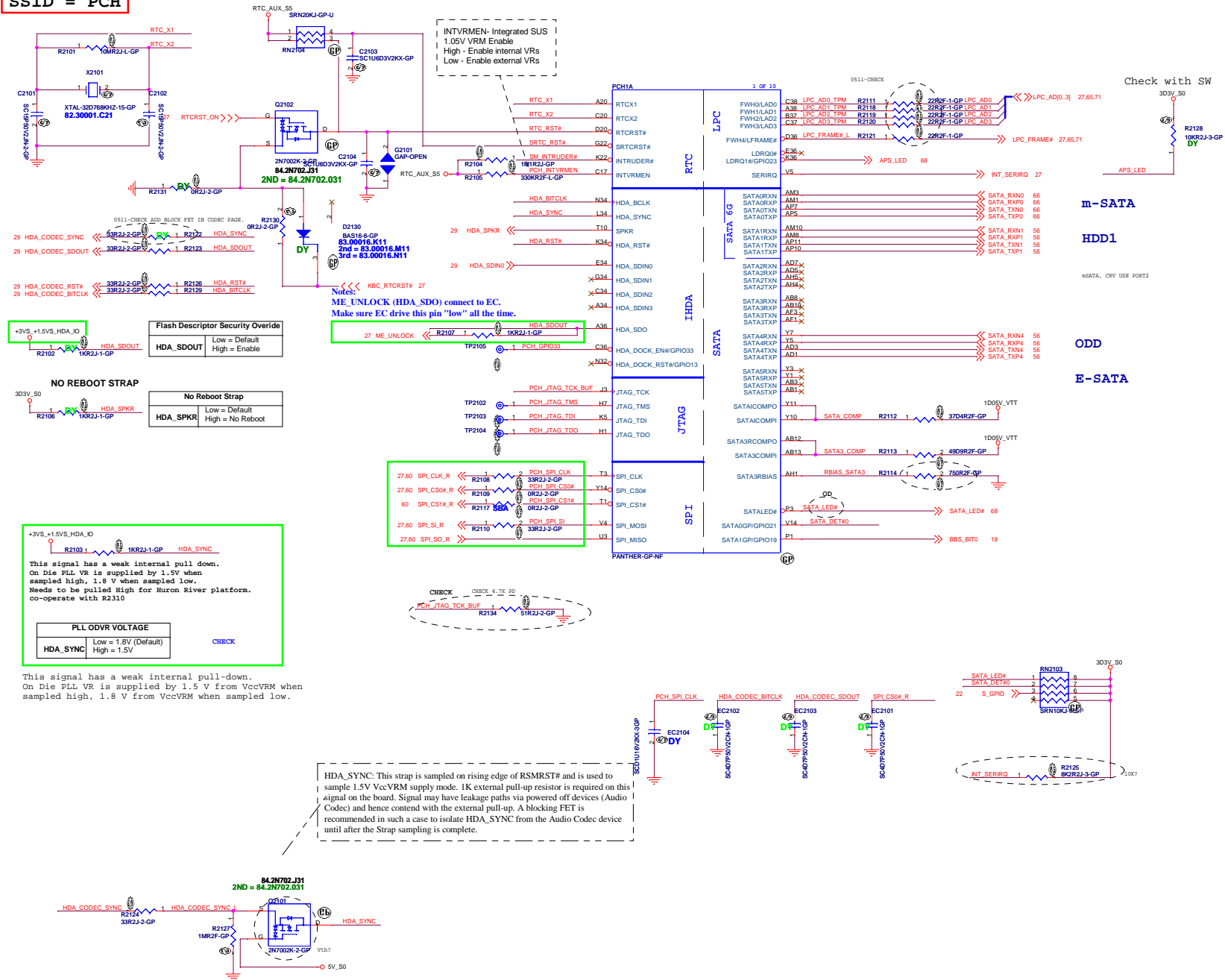
<Core Design>

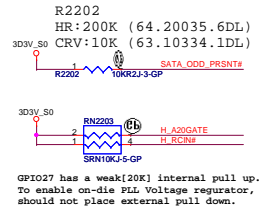
SSID = PCH

If PCIE port 1 is disabled, it will cause all PCIE port disabled



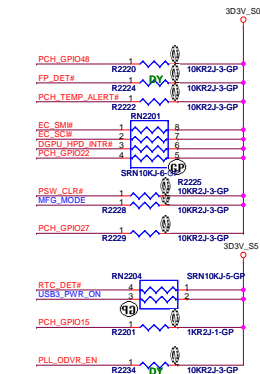
SSID = PCH



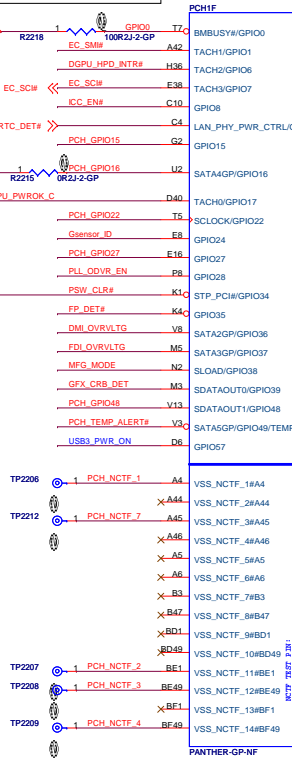
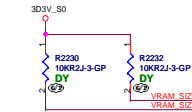
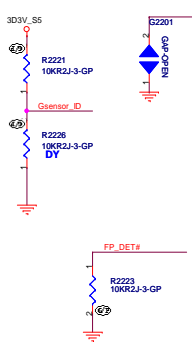
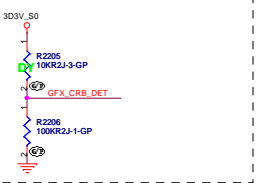


Note:
For PCH debug with XDP, need to NO STUFF R2218

G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY

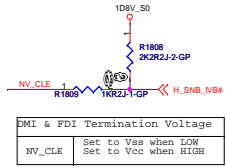
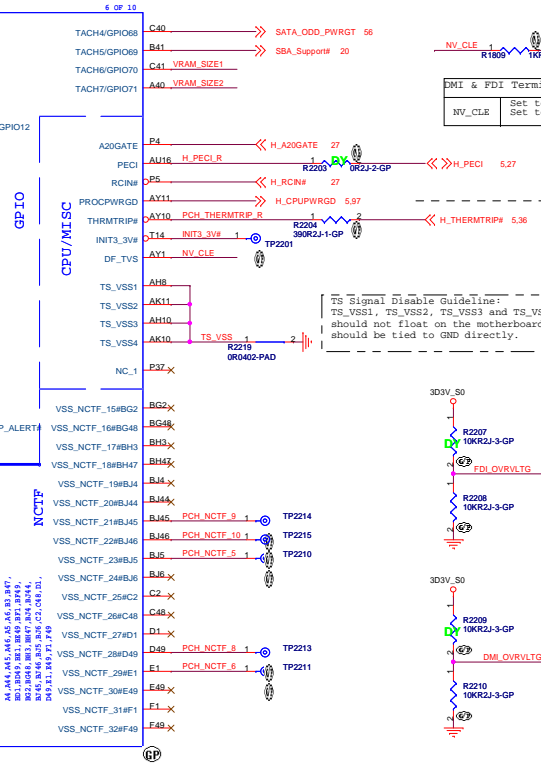


	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

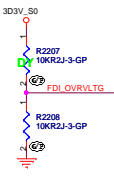


PLL ON DIE VR ENABLE

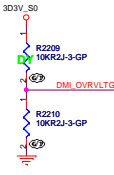
NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 INSTALLED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

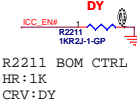


DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLGT)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

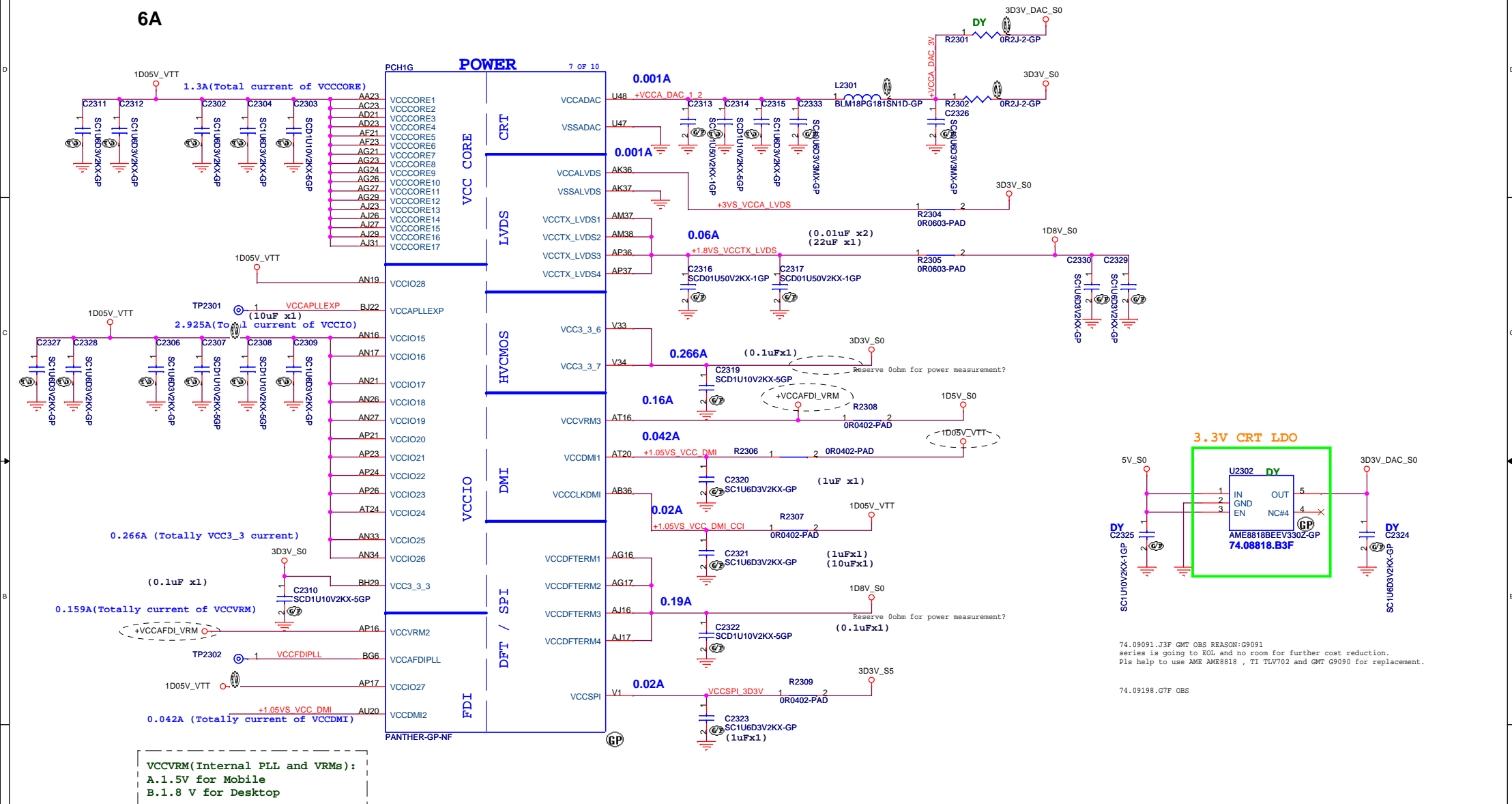
Integrated Clock Chip Enable	
IOC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.



SSID = PCH

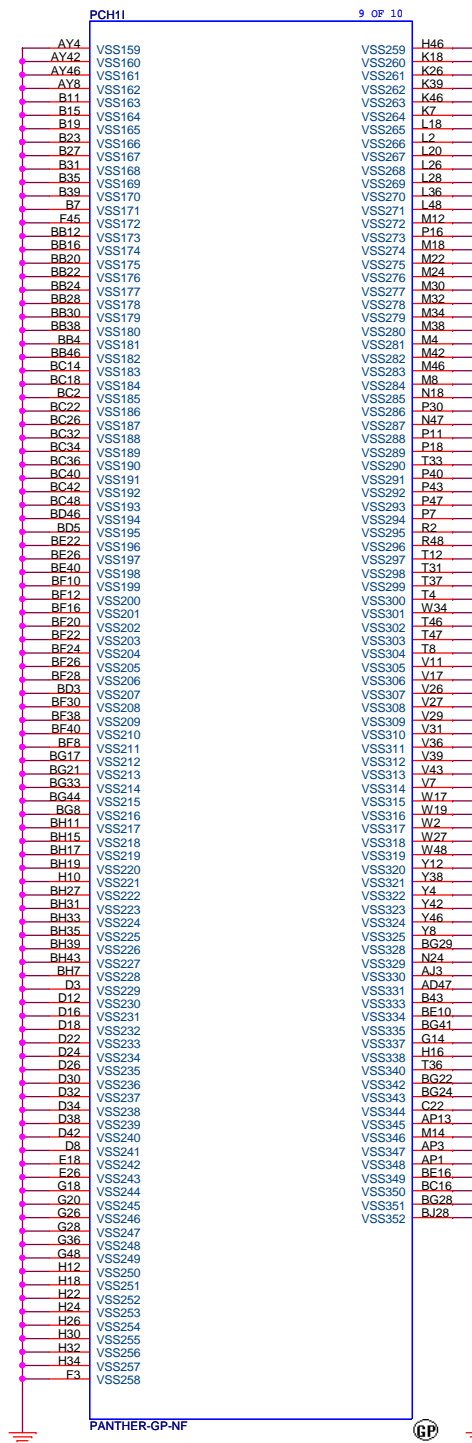
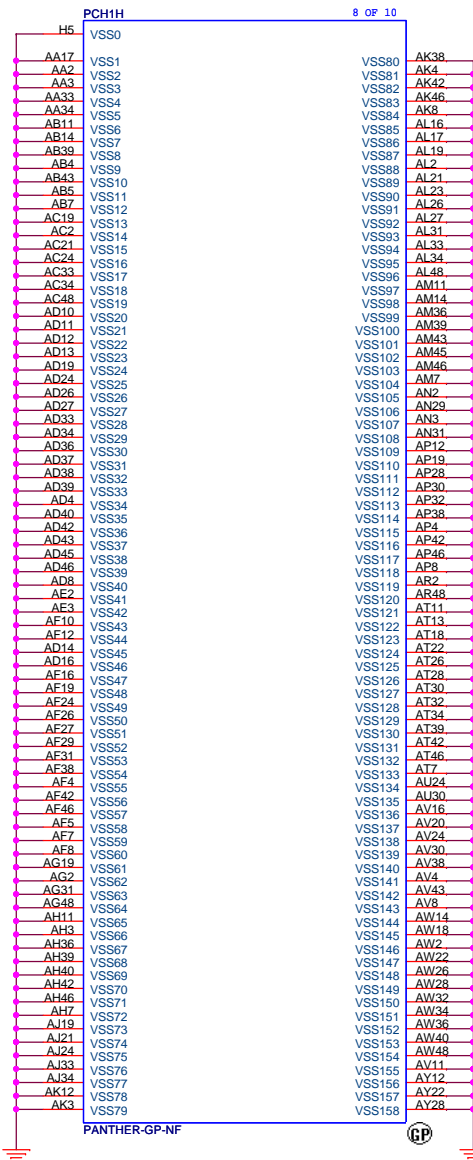
6A



<Core Design>

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Title		
PCH : POWER1		
Size	Document Number	Rev
A3	LA480	SD
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SSID = PCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

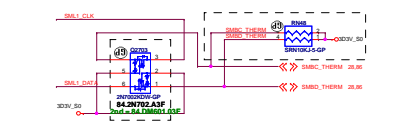
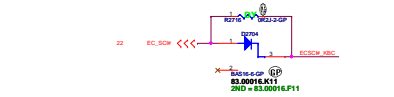
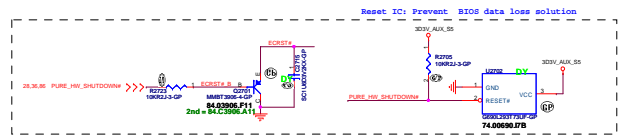
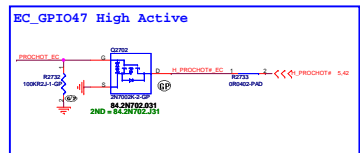
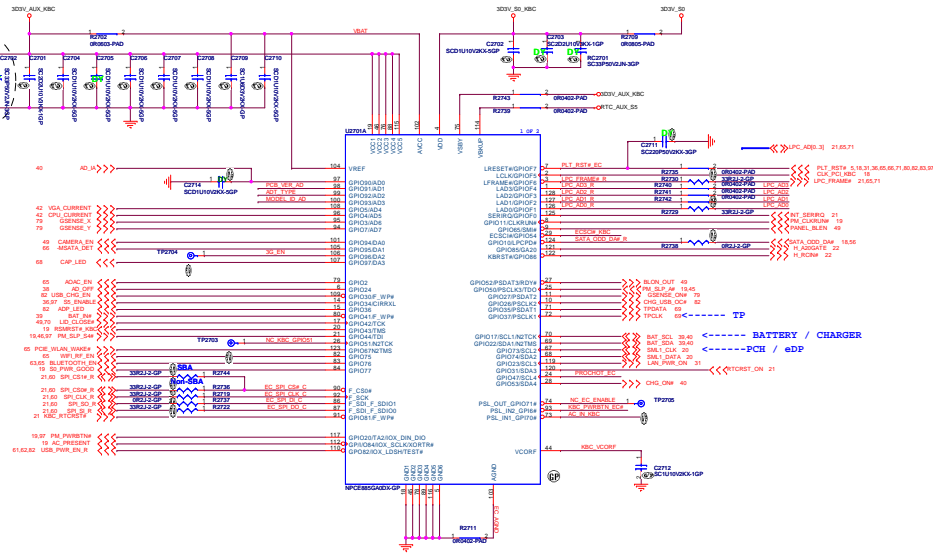
Title			PCH : VSS	
Size	Document Number	Rev		SD
A3	LA480			
Date:	Friday, January 06, 2012	Sheet	25	of 103

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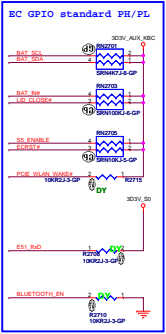
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>Reserved</div>	
Size <div>A4</div>	Document Number <div>LA480</div>
Date <div>Friday, January 06, 2012</div>	Rev <div>SD</div>
Sheet 26 of 103	

SSID = KBC



MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA	100.0K	33.0K	2.481V
OPTIM08	100.0K	47.0K	2.245V



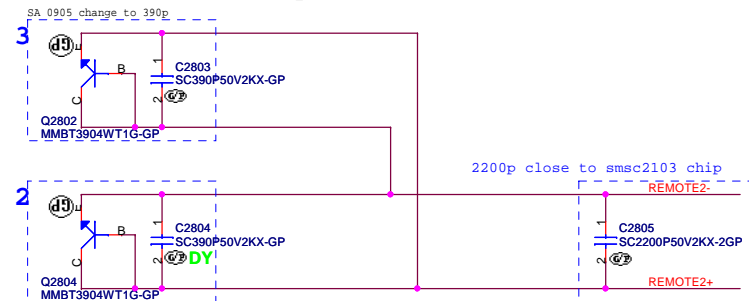
PCB Version A/B (Pin98)	Pull-Low Resistor	Pull-High Resistor (3.0V_AUX_S5)	Voltage (Pin98)
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
+L	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

SSID = Thermal

Thermal sensor

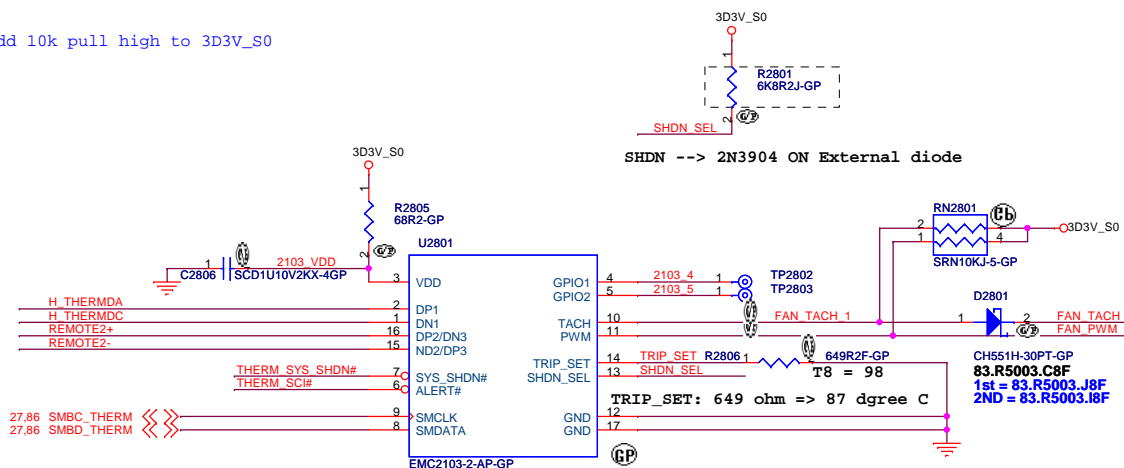
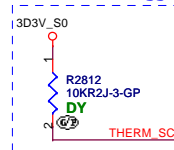
Close to SO-DIMM on top side.



between CPU, VGA and DIMM on bottom side

20110718_Carrey:

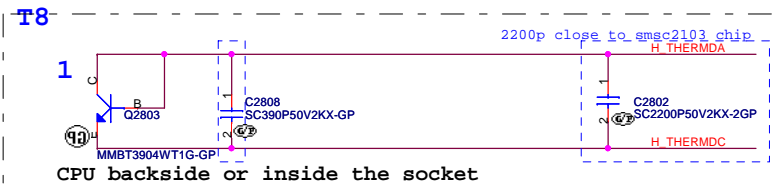
For Vendor suggestion, add 10k pull high to 3D3V_S0



pin6, ALERT# OD
pin7, SYS_SHDN# OD

20110718_Carrey:

For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803

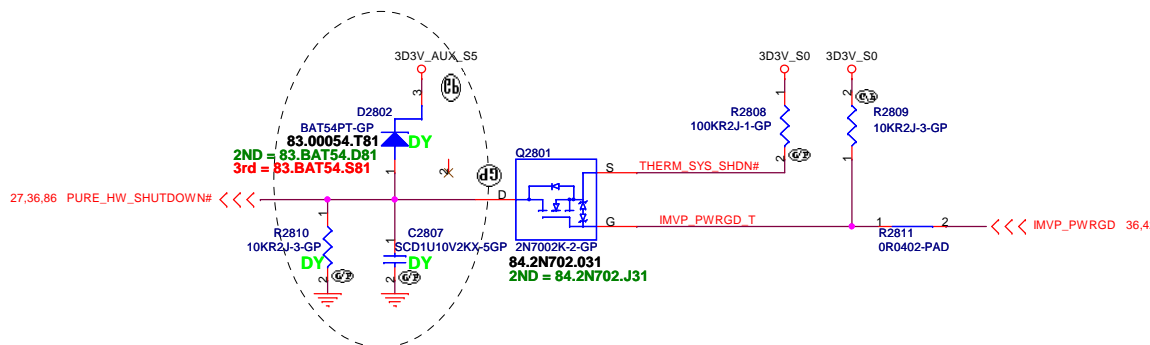
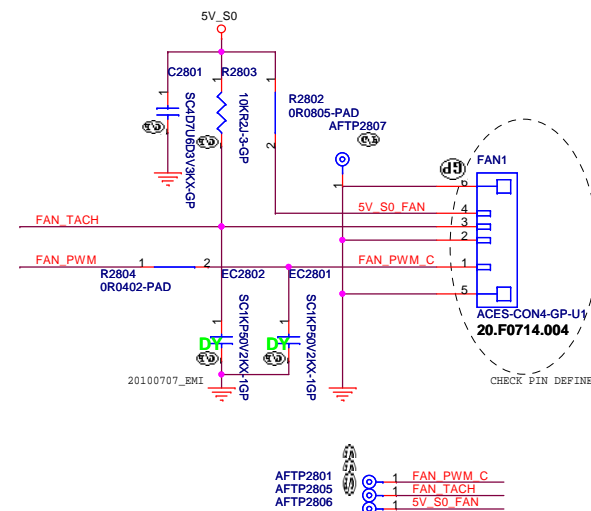


CPU backside or inside the socket

CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit



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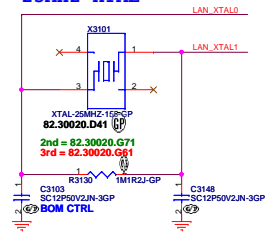
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THERMAL SENSOR SMSC EMC2103		
Size	Document Number	Rev
A3	LA480	SD
Date: Friday, January 06, 2012		
Sheet 28 of 103		

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<Core Design>

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Title			
Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 30 of	103

25MHz XTAL

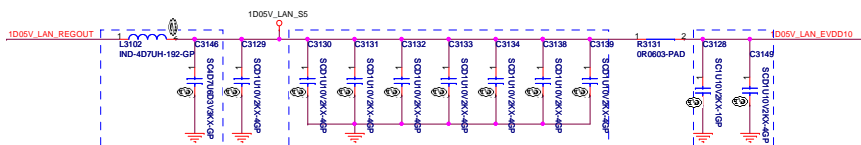
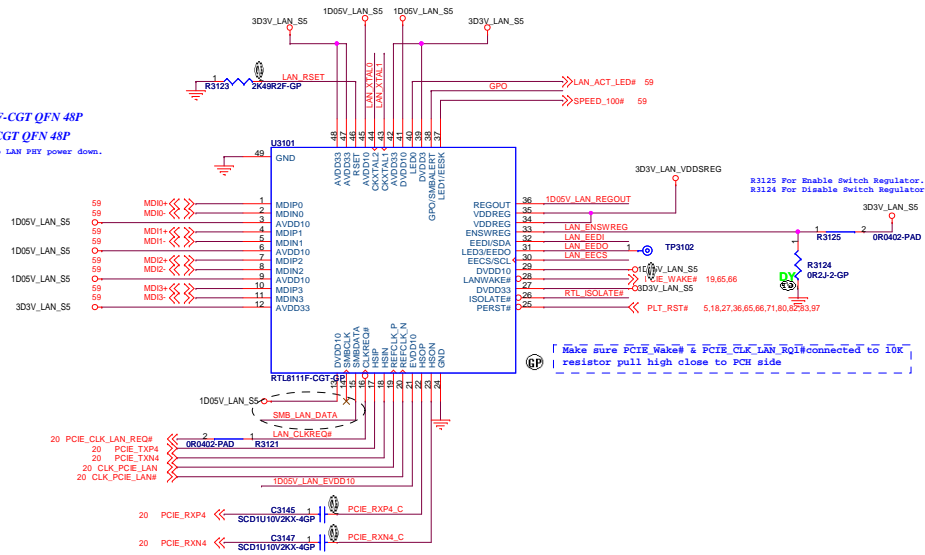


	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

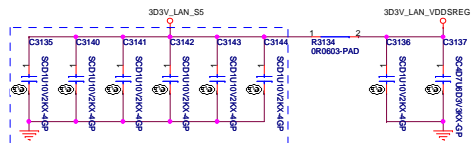
8111F can use GPIO to inform system to do LAN PHY power down.



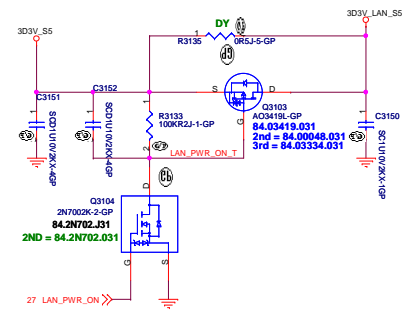
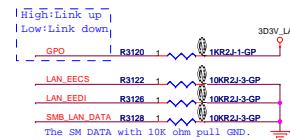
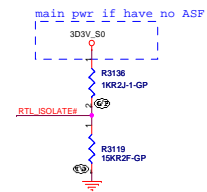
L3102 adopt spec
C3104 change to
type capacitor

Layout Note: Close to U3101 pin C3130 - C3134,C3138,C3139
For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149
Close to U3101 pin21



Layout Note: C3135, C3140~C3144 Close to U3101 pin
For VDD33 pins - 12, 27, 39, 42, 47, 48.



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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 33 of	103

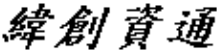
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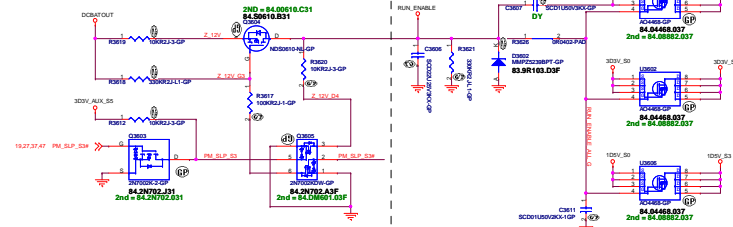
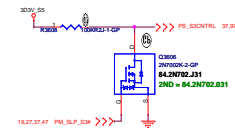
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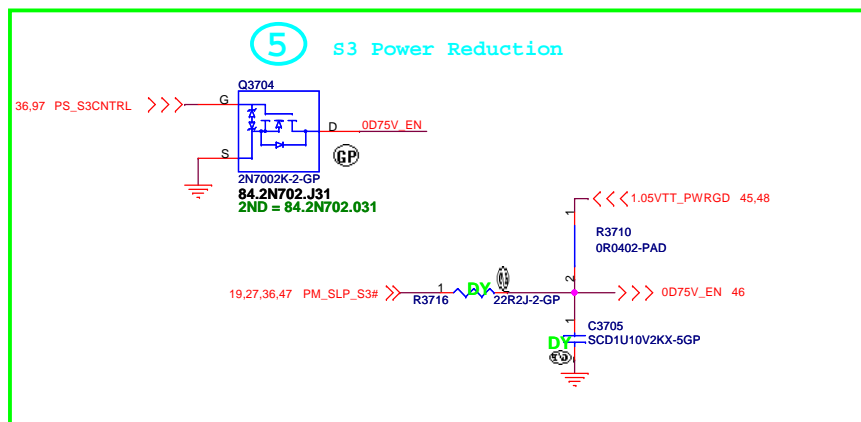
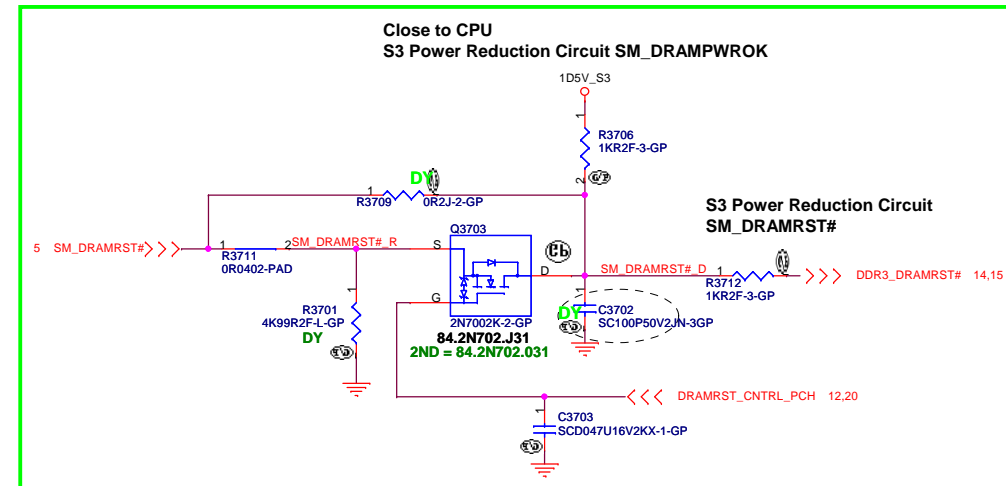
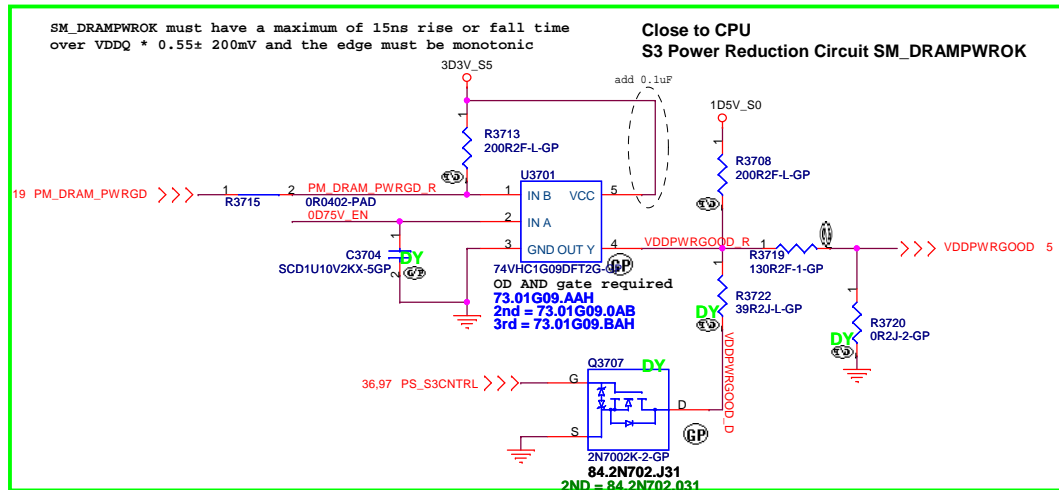
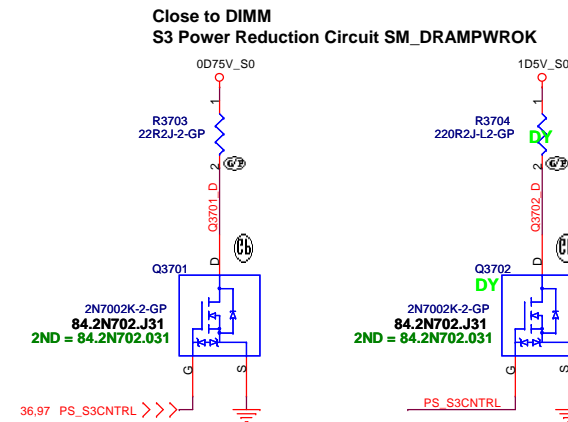
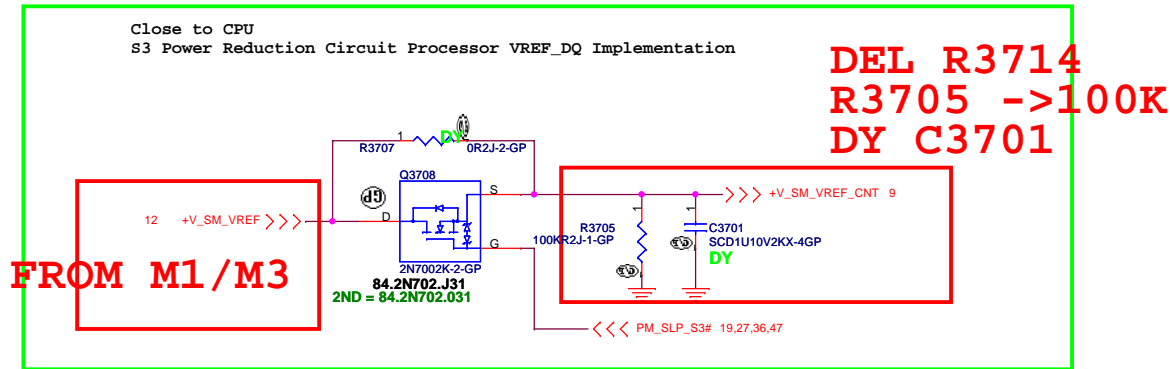
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 34 of	103

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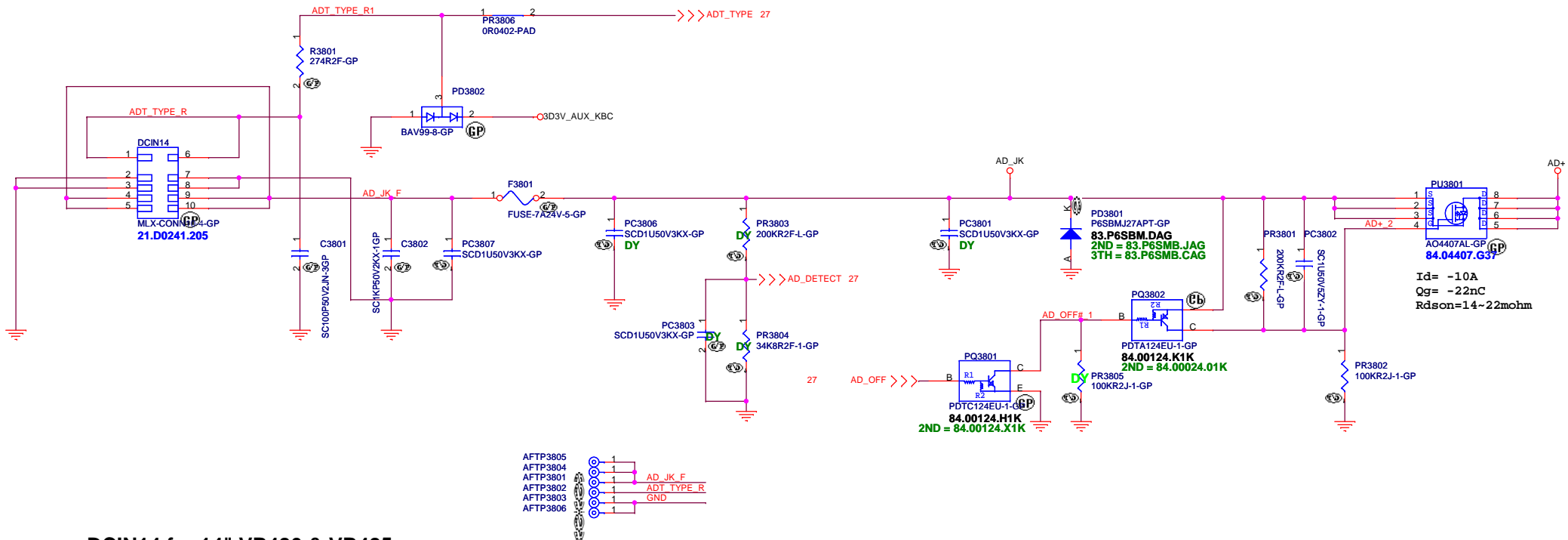
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Title			
USB 3.0 Controller			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 35 of	103

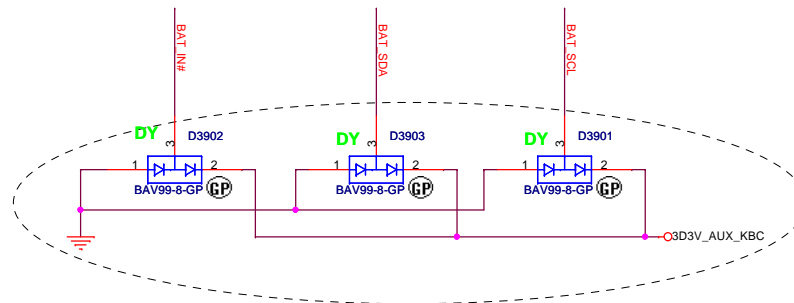
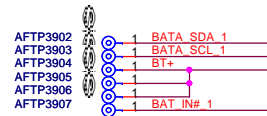
[illegible][illegible]



Adaptor in to generate DCBATOUT



Swap for v480



<Core Design>

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Title				BATT_CONN			
Size	Document Number						Rev
	LA480						SD
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SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k	100K
120w	64.40425.6DL	100K

STOP_CHG#
connects to KBC

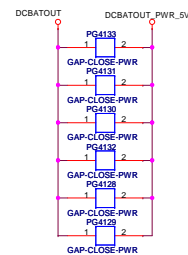
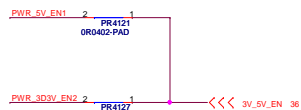
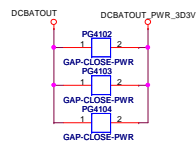
Charger Current=1.4~3.6A

<Core Design>

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File	<Title>	Rev
Size	Document Number	SD
A2	LA480	
Date:	Friday, January 06, 2012	Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=5.25A
OCP>7.8A

Cyntec. 2.2uH 7.3*6.3
DCR=18~20mohm
Idc=8A, Isat=14A

Id=12A, Qg=3.8nC,
Rdson=24~30 mohm

Id=12A, Qg=3.8nC,
Rdson=24~30 mohm

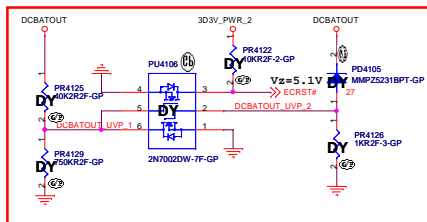
Design Current=5.25A
OCP>7.8A

Cyntec. 3.3uH 6.5*6.9*3
DCR=28~30mohm
Idc=6A, Isat=13.5A

Id=16A, Qg=7.3nC,
Rdson=13.5~16.5 mohm

Close to VFB Pin (pin2)

Close to VFB Pin (pin5)



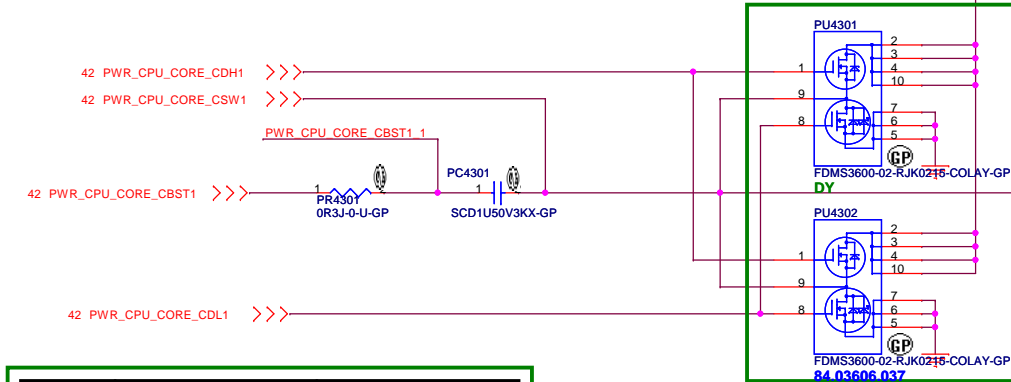
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshui,
Taipei Hsien 221, Taiwan, R.O.C.

Title TPS51123_5V_3D3V

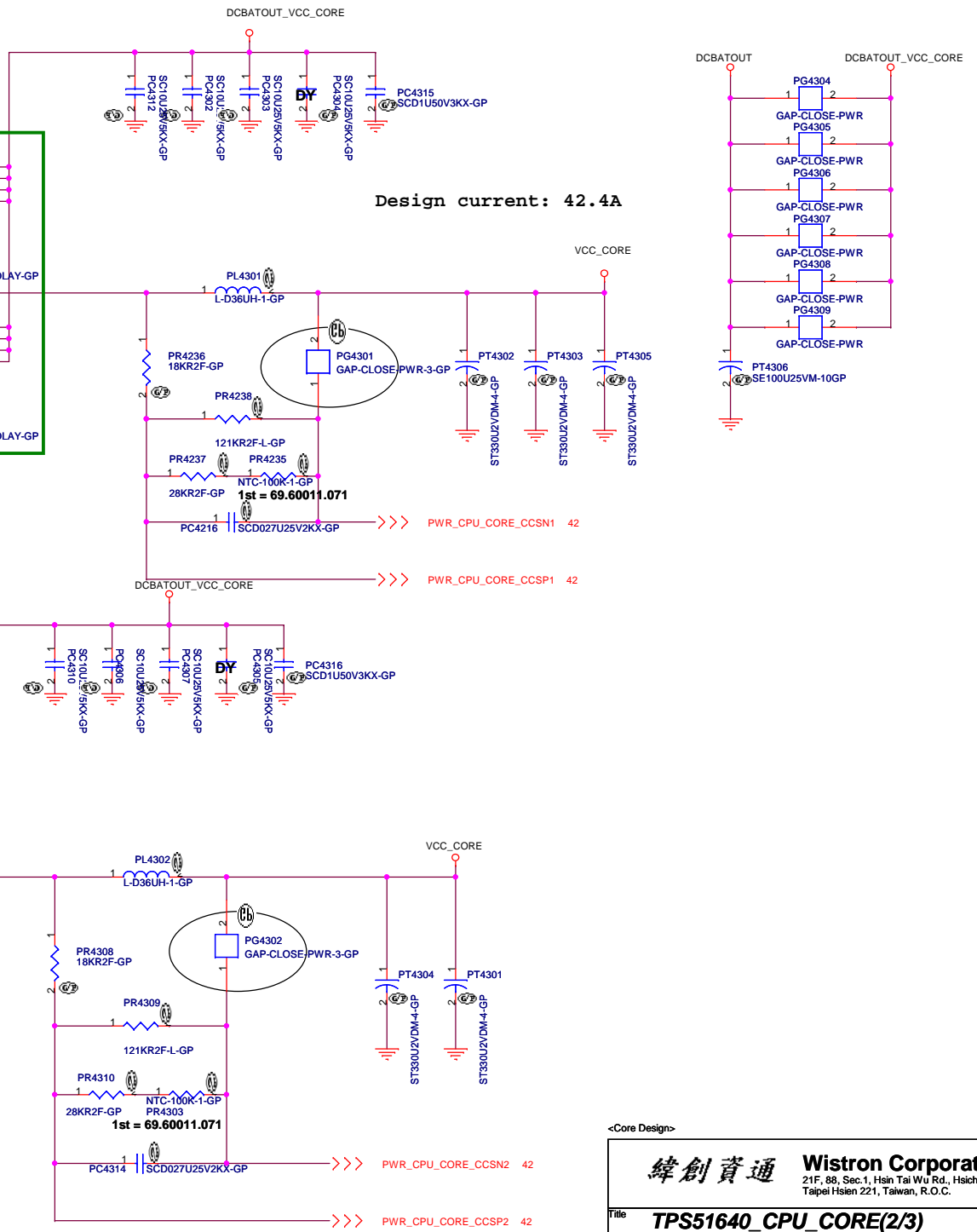
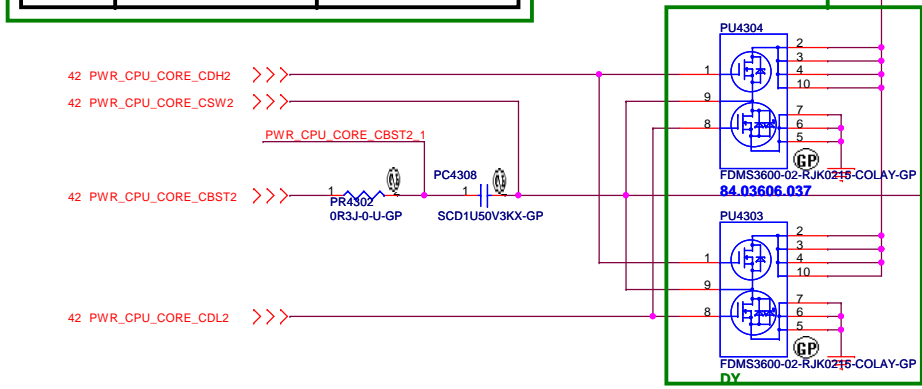
Size Document Number Rev SD

Date: Friday, January 08, 2012 Sheet 41 of 104

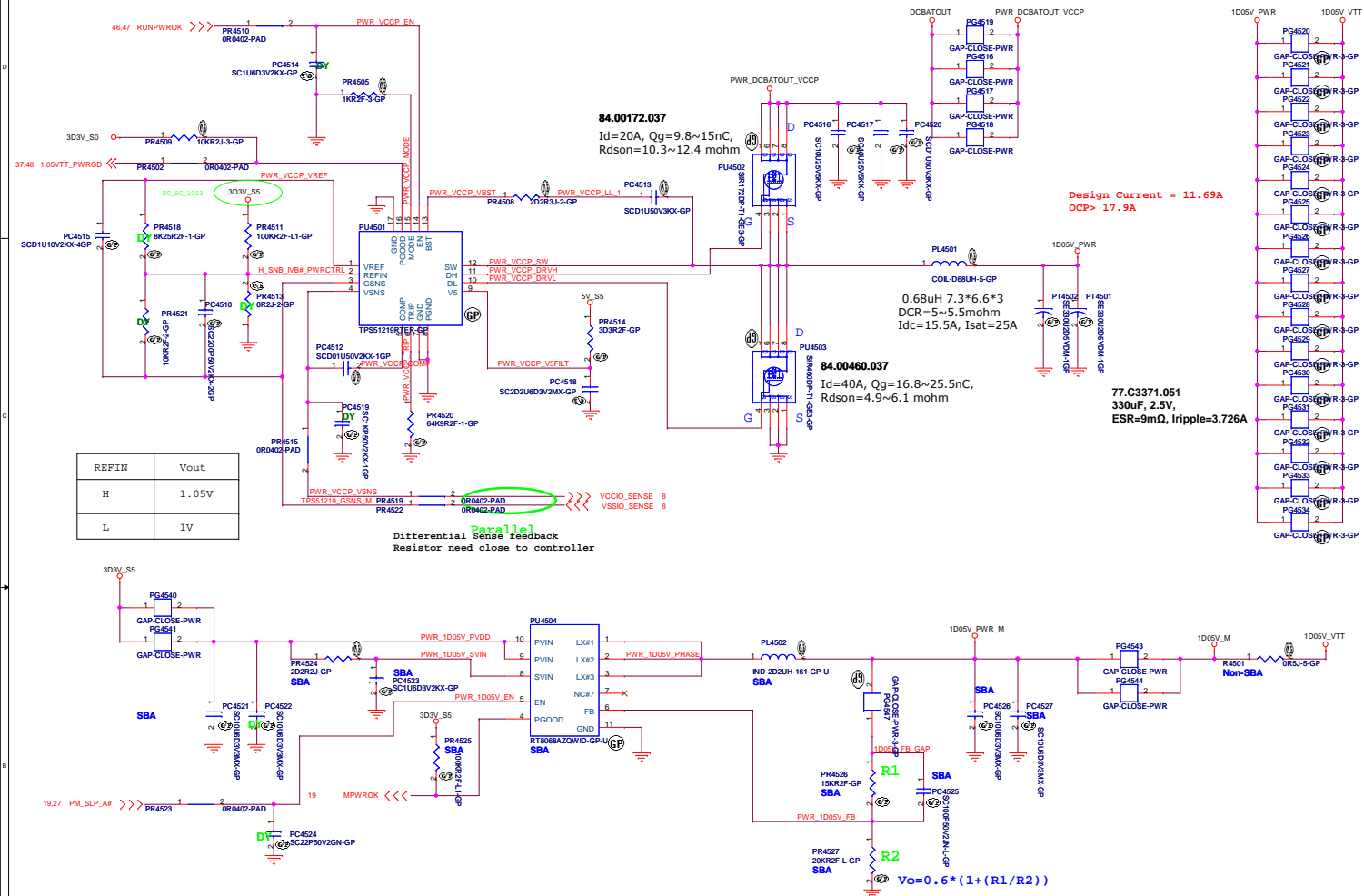


	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

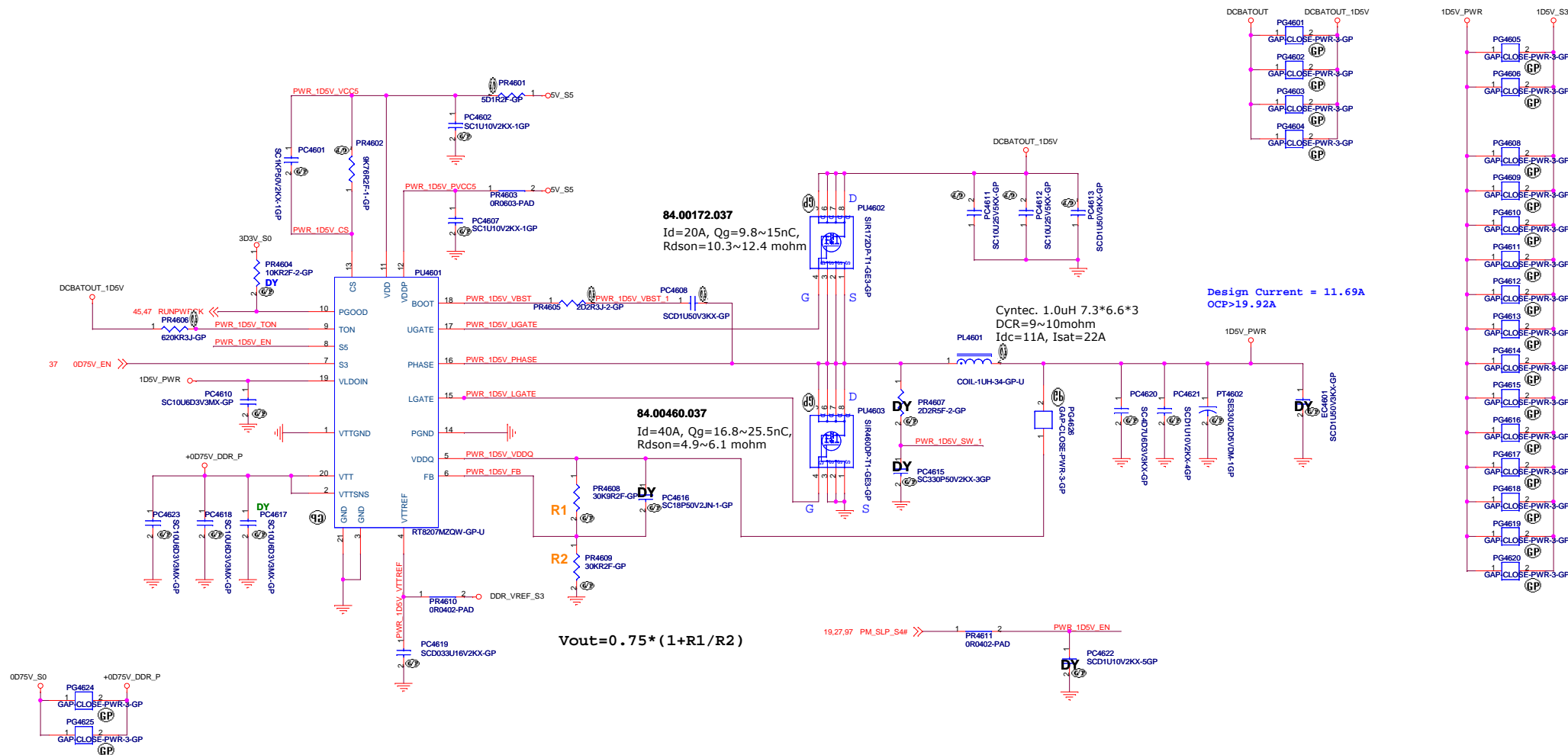
BOM control



Design current: 42.4A

TPS51219 for 1D05V

	A	
SSID = PWR.Plane.Regulator_1p5v0p75v		



◀Core Design▶

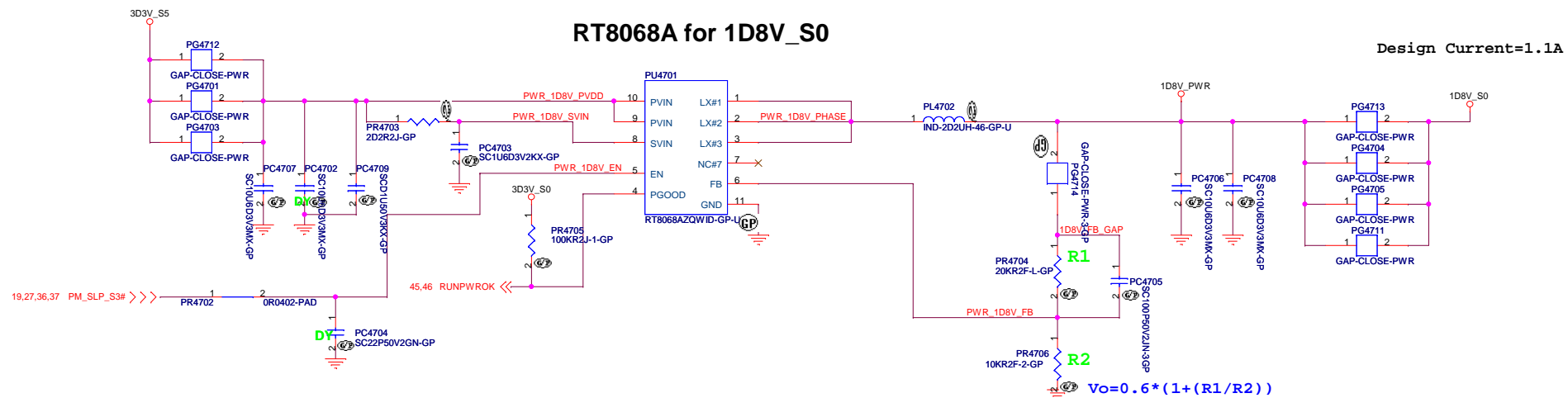
緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8207M 1D5V 0D75V
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Size	Document Number	<Doc>	Rev
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Date:	Friday, January 06, 2012	Sheet	46	of	103
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SSID = PWR.Plane.Regulator_1p8v



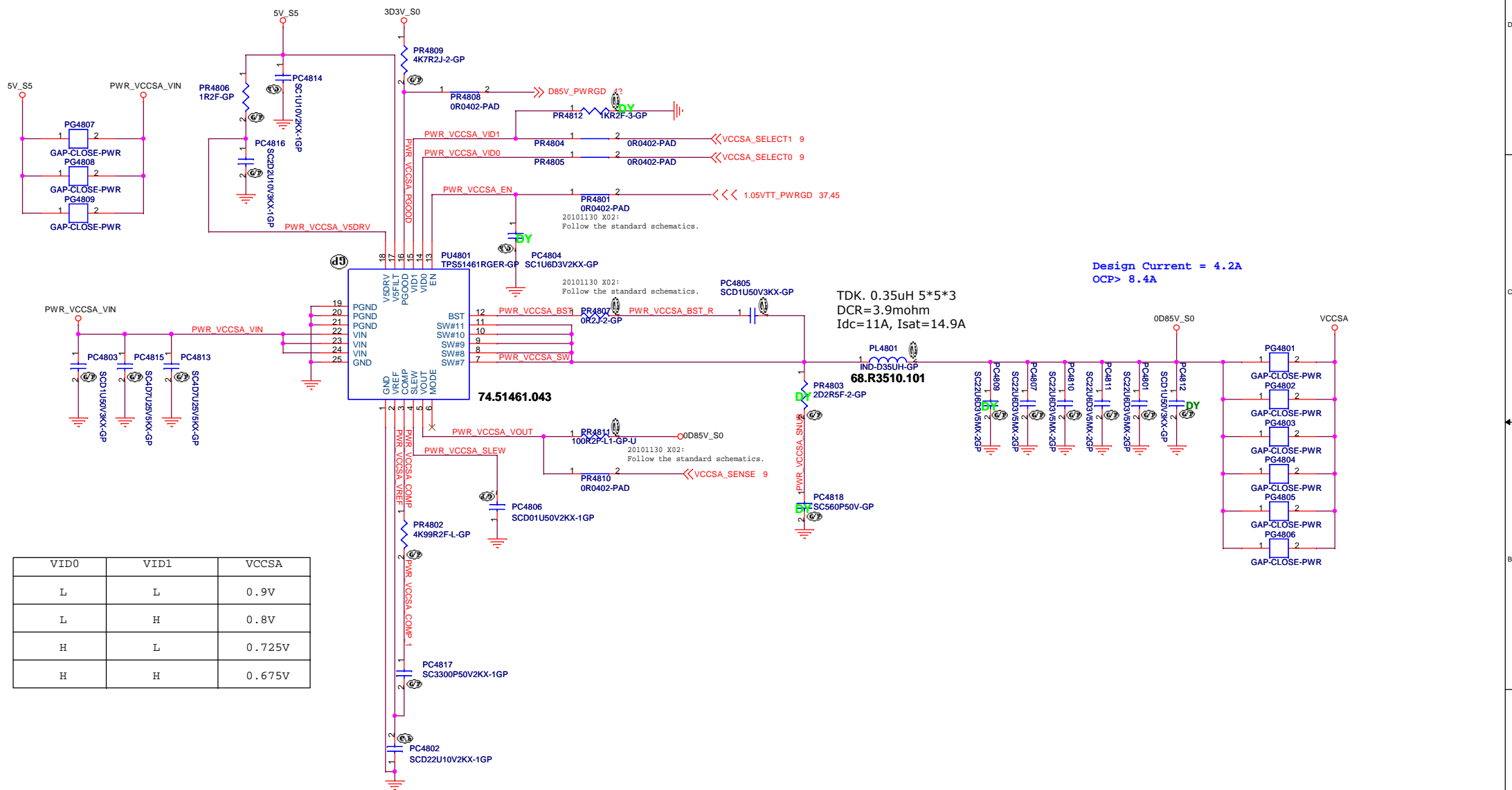
<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title			PWM_1D8V_RT8015B		
Size	Document Number				Rev
Date:	Friday, January 06, 2012				SD
Sheet	47	of	103		

TPS51461 for VCCSA



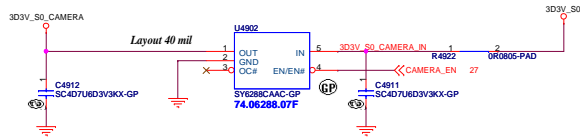
VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

SSID = VIDEO

LVDS connector

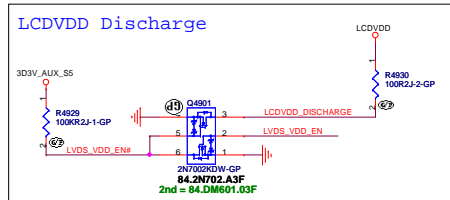
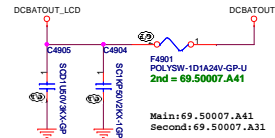
LCD / Inverter Connector

CAMERA POWER

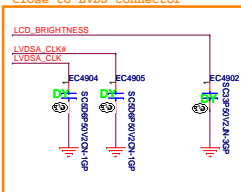


SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

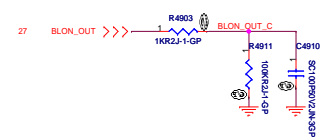
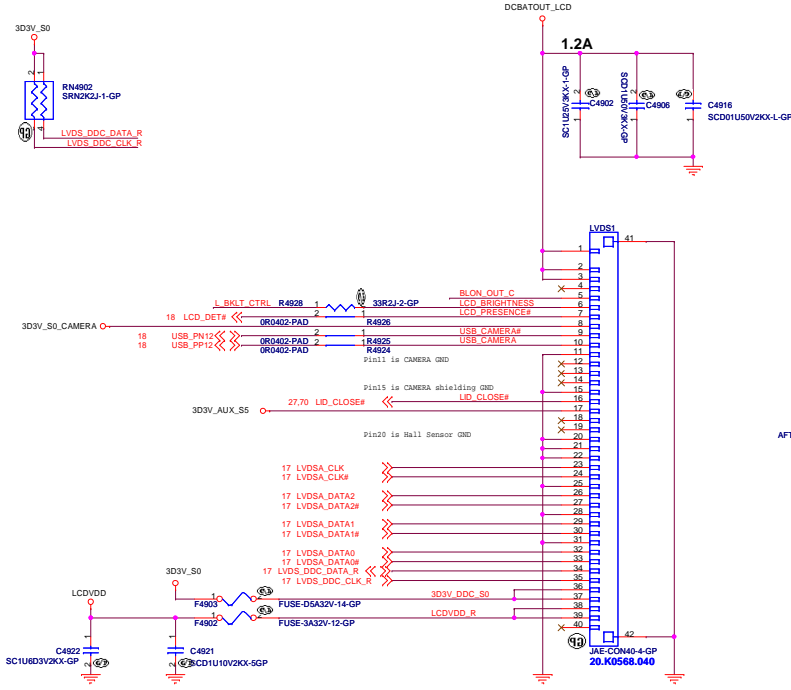
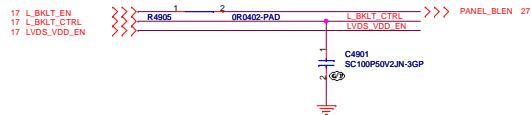
LCD POWER



For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En

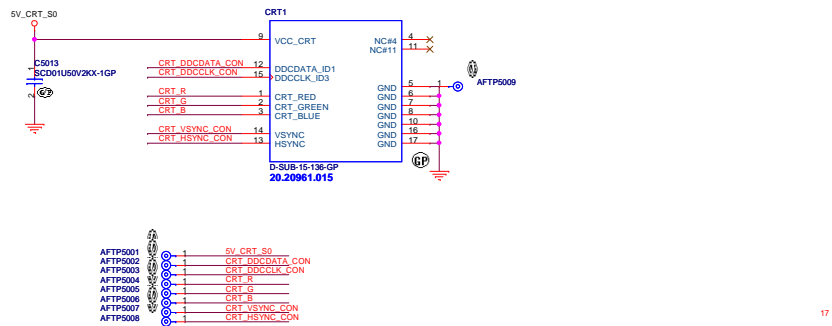


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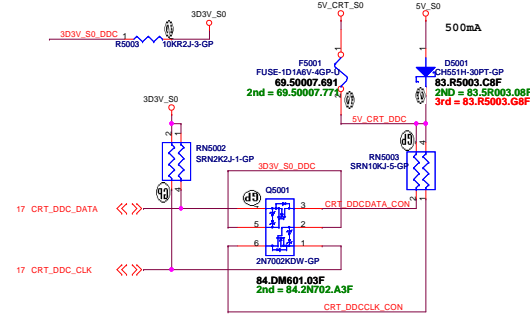
File	LCD Connector		
Size	Document Number	Rev	SD
A2	LA480		
Date:	Friday, January 06, 2012	Sheet	48 of 103

CRT connector

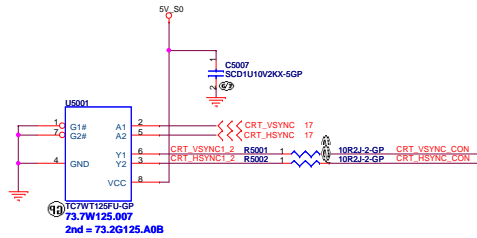


CRT DDCDATA & DDCCLK level shift

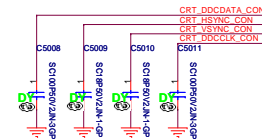
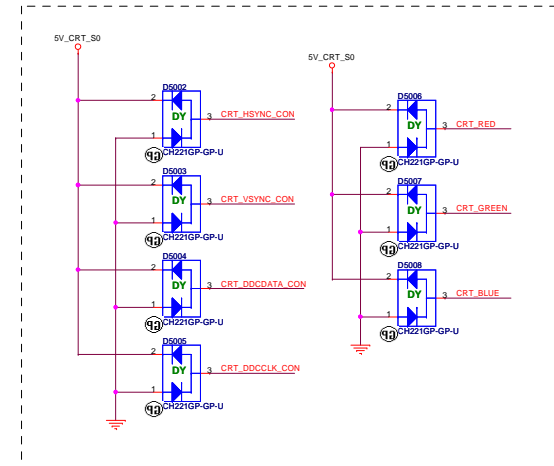
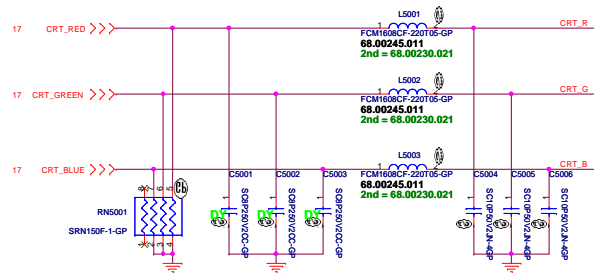
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



CRT RGB



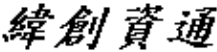
<Core Design>

緯創資通 Wistron Corporation
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File			Rev
CRT Connector			SD
Size	Document Number		
A2	LA480		
Date	Friday, January 06, 2012	Sheet	60 of 103

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
eDP			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 52 of	103

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
S-VIDEO			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 53 of	103

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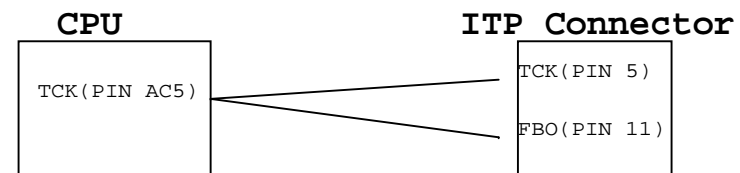
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 54 of	103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size
A4

Document Number

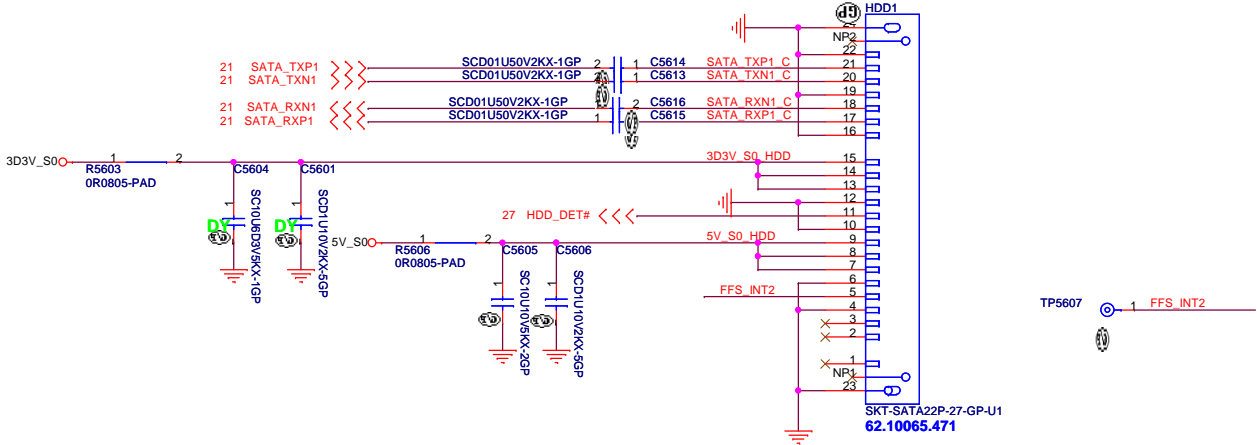
LA480

Rev
SD

Date: Friday, January 06, 2012

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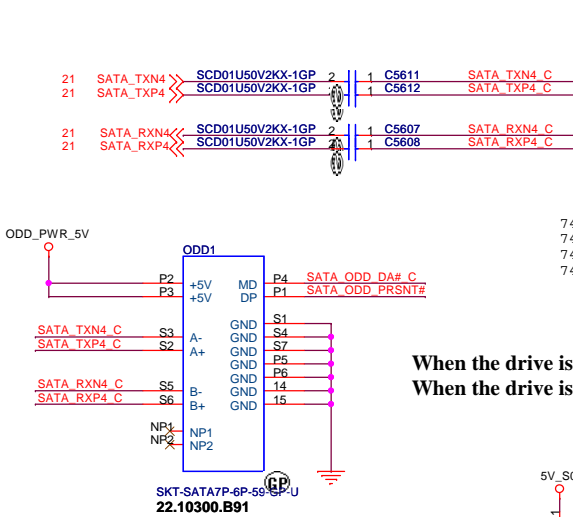
SATA HDD Connector



ODD Connector

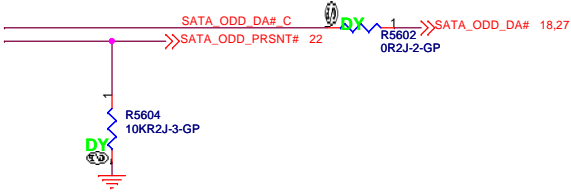
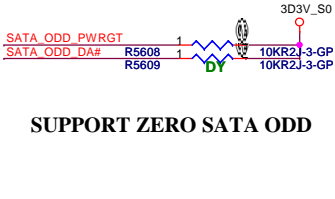
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



- 74.02069.079 TI TPS2069DGNR MSOP 8P
- 74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
- 74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
- 74.07534.A79 UPI UP7534ARA8-15 MSOP8P

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD

Current limit
Active High
typ =>2A

TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

<Core Design>

緯創資通 Wistron Corporation

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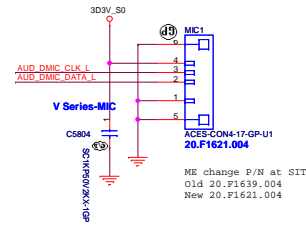
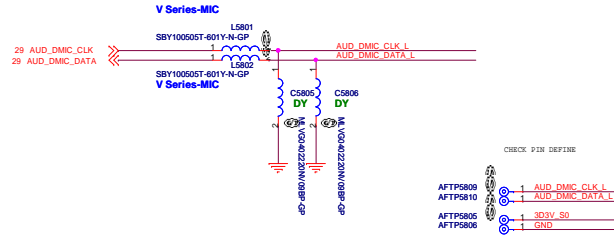
Title		HDD/ODD	
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	56 of 103

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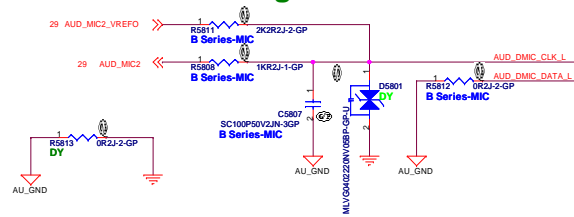
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>E-SATA+USB</div>		
Size <div>A4</div>	Document Number <div>LA480</div>	Rev <div>SD</div>
Date: Friday, January 06, 2012		Sheet 57 of 103

Int. Digital MIC for V series



Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS

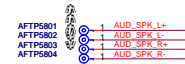
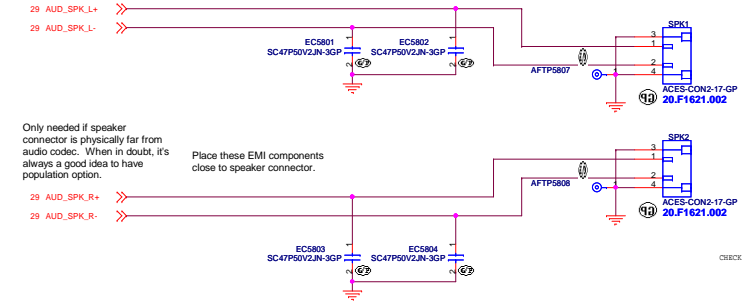


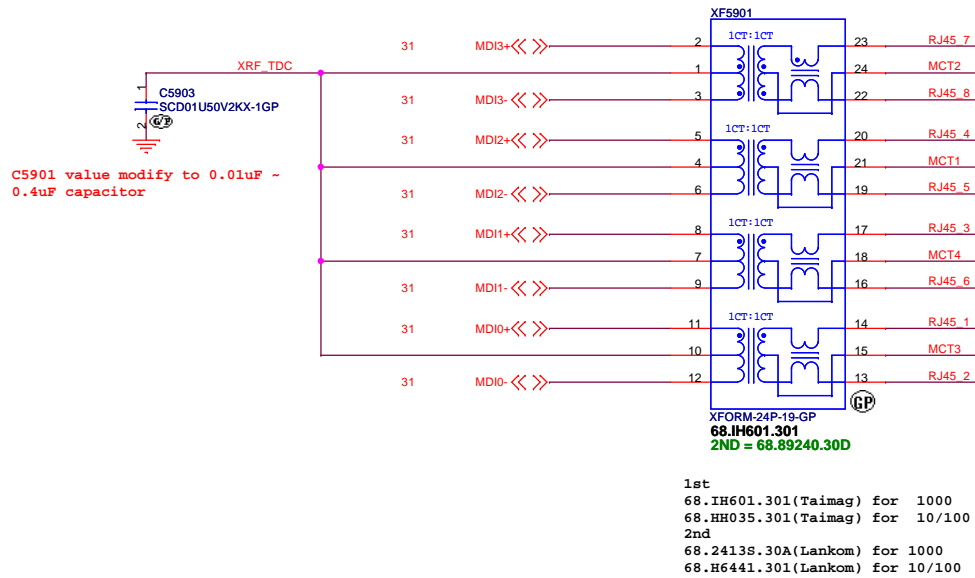
Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

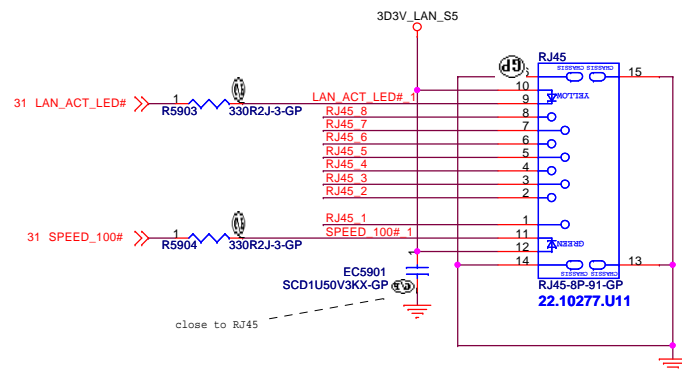
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緯創資通 Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Audio Jack	
Size A2	Document Number
LA480	Rev SD
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GIGA Lan Transformer



LAN Connector



TVS

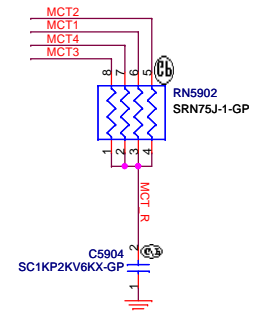
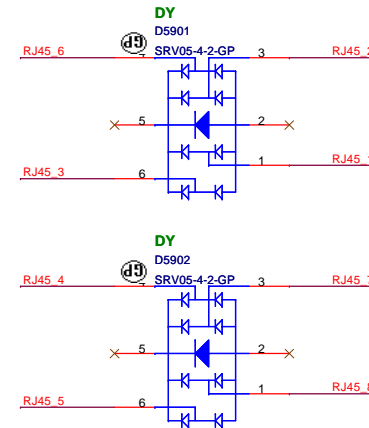
83.00005.BAE

DIODE ARR SRV05-4.TCT SOT-23-6

83.09904.AAE

DIODE ESD AZC099-04S SOT23-6L

Swap for v480



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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page	Page	

RJ45 / TransformerSize
A3

Document Number	
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LA480

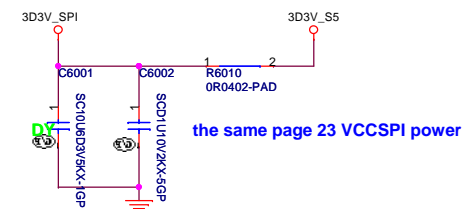
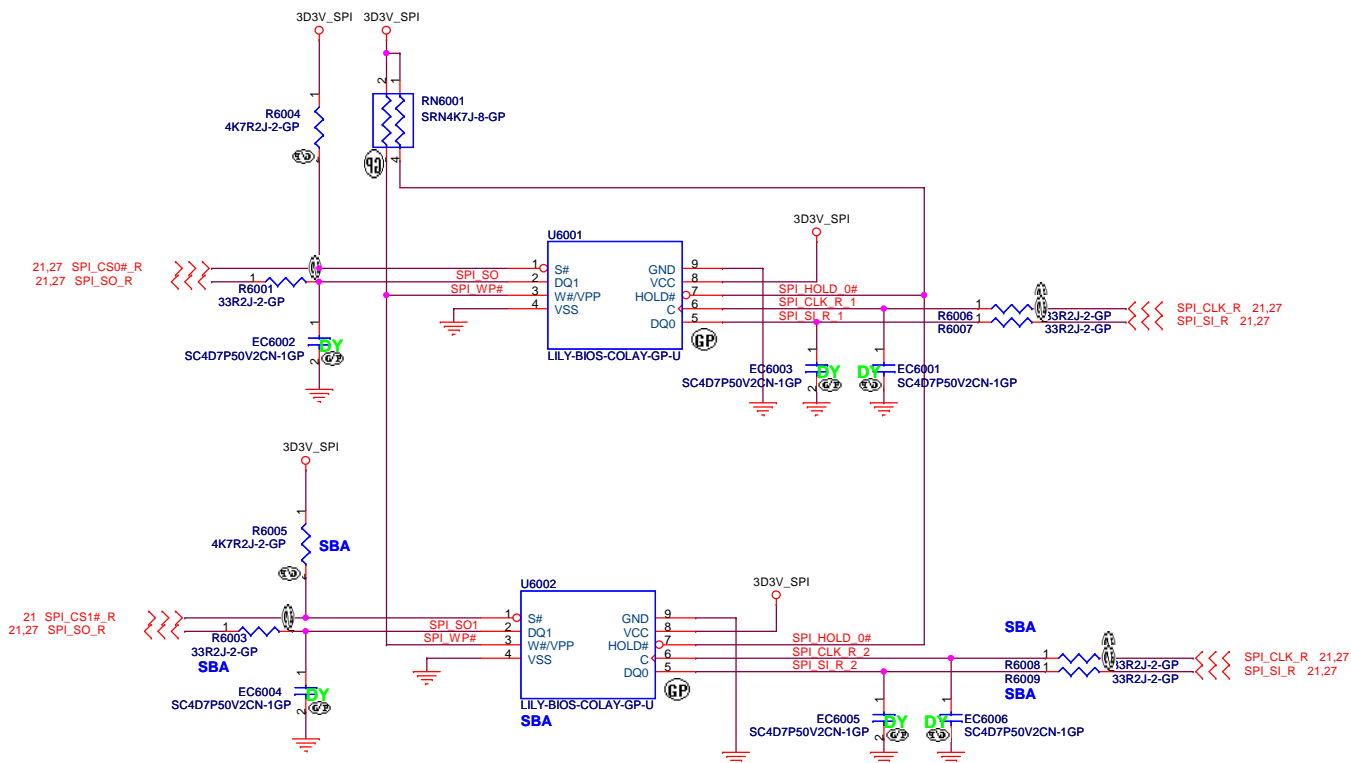
Rev
SD

Date: Friday, January 06, 2012

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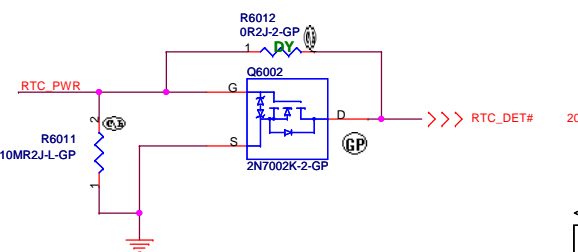
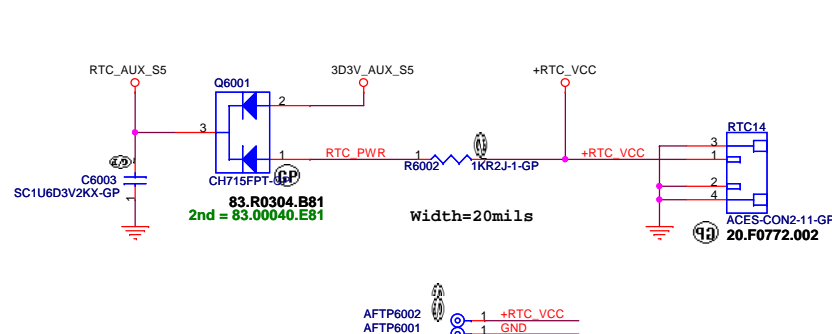
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



4MB			
SO8	Marconix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marconix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSO8	Marconix	MX25L12836EZNI-10G	72.25128.X01
	Marconix	MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT

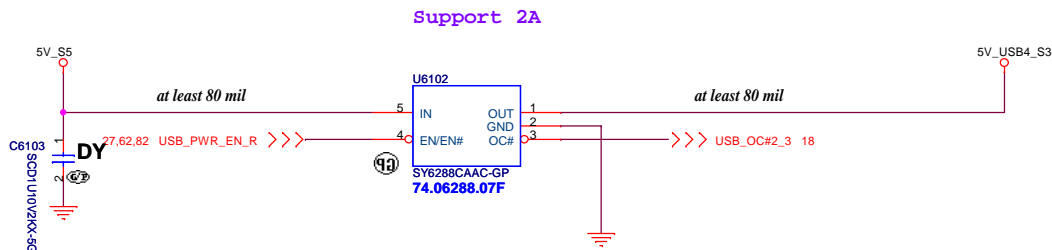


<Core Design>

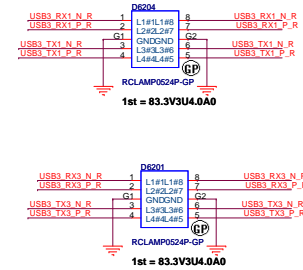
緯創資通 Wistron Corporation
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Title			Flash/RTC
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	60 of 103

USB Board CONN.

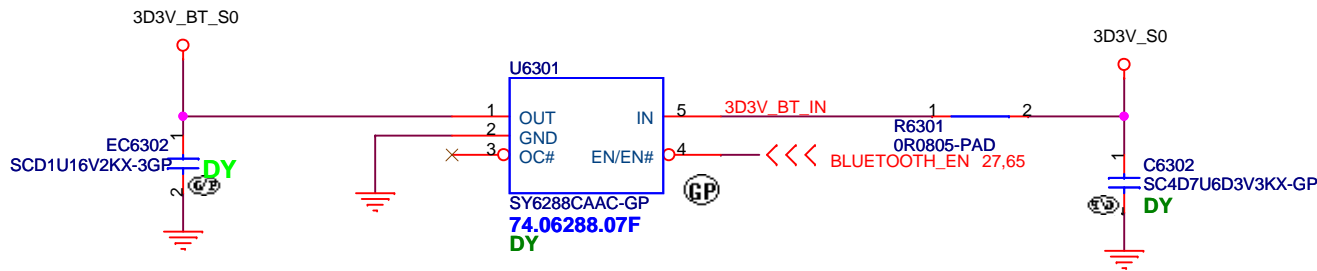


USB3.0 Port4



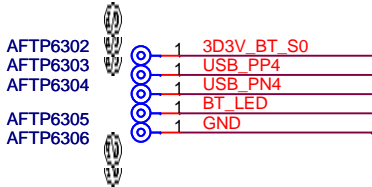
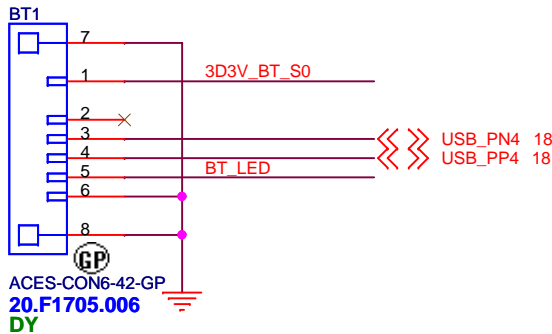
SSID = User.Interface

Bluetooth conn.



BT Module pin definition is same as LA470

SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active



<Core Design>

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Title

Bluetooth

Size

Document Number

Rev

A4

LA480

SD

Date

Friday, January 06, 2012

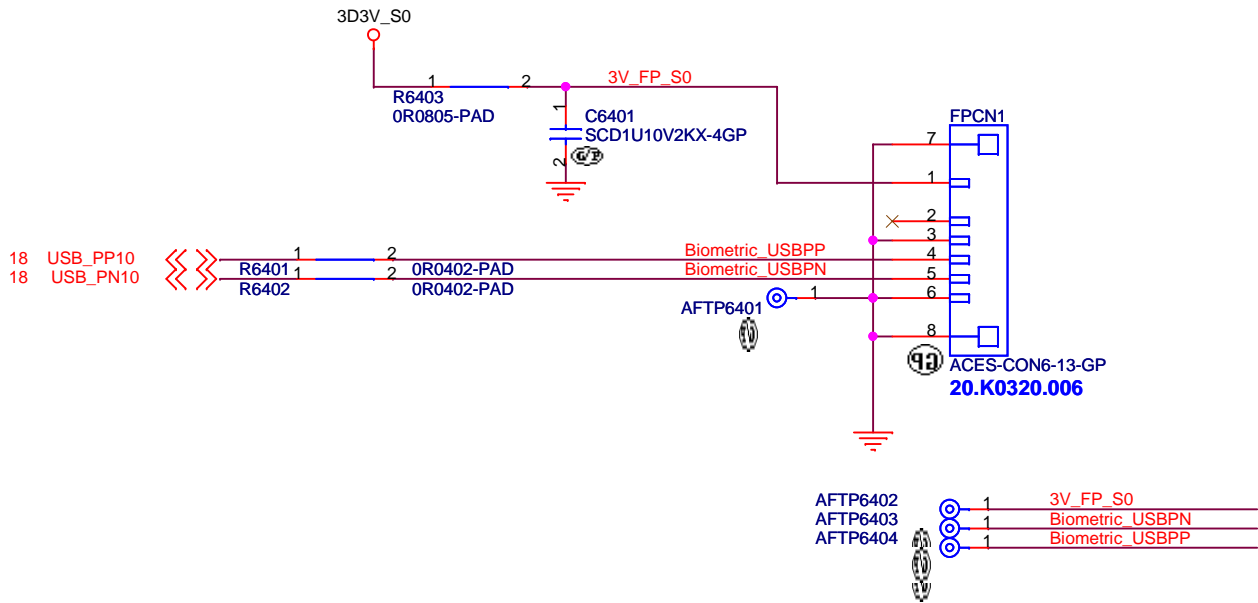
Sheet

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of

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Finger Printer Connector



<Core Design>

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Title

Finger Printer Connector

Size
A4

Document Number

LA480

Rev

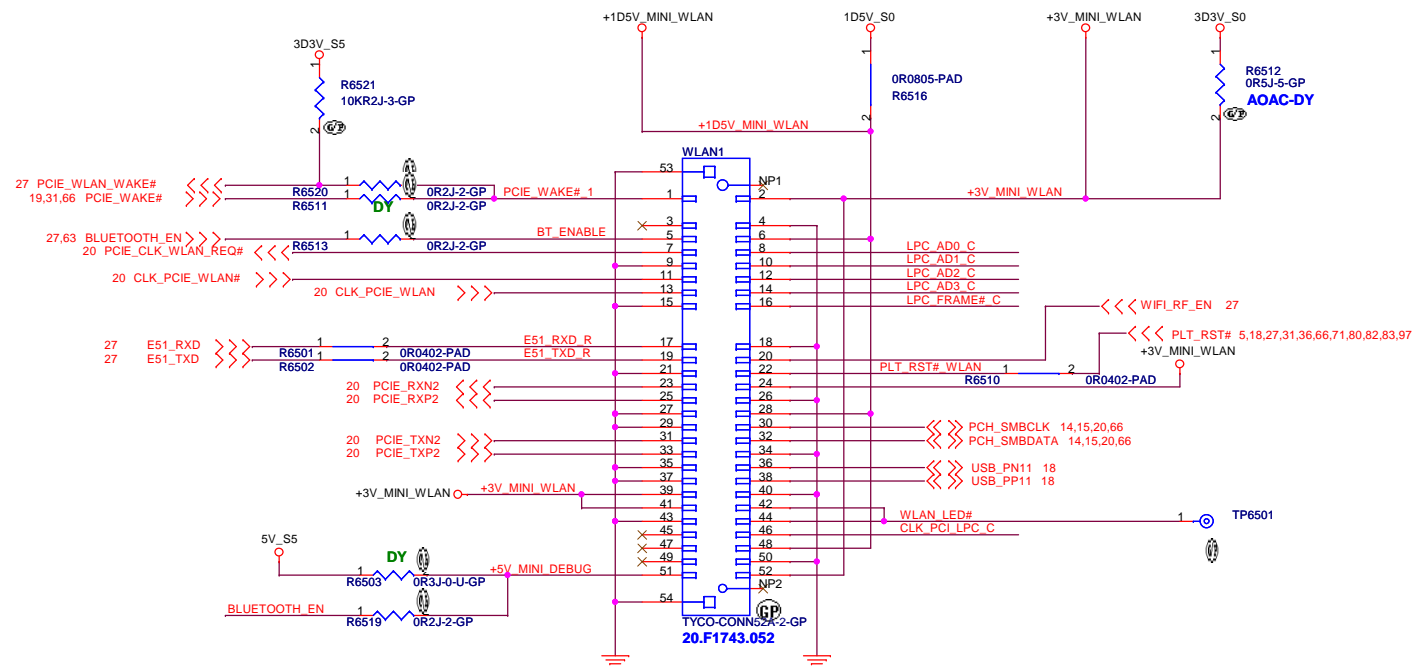
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Date: Friday, January 06, 2012

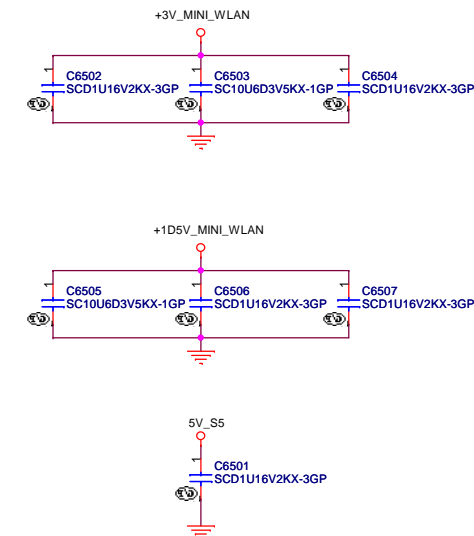
Sheet 64 of 103

SSID = Wireless

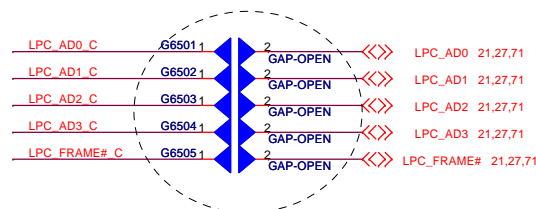
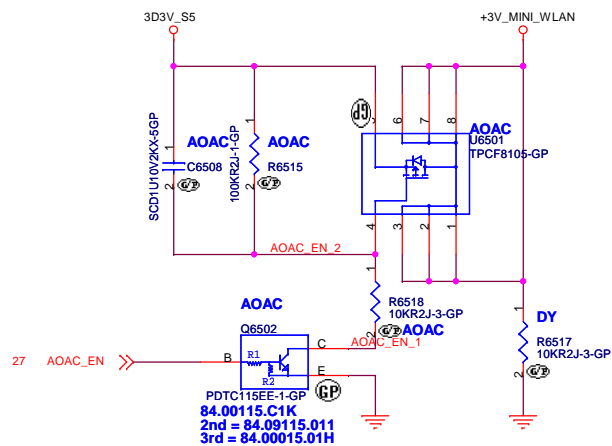
Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN



Reserve for AOAC



G6506~G6511
placement close close WLAN1
in bottom side

<Core Design>

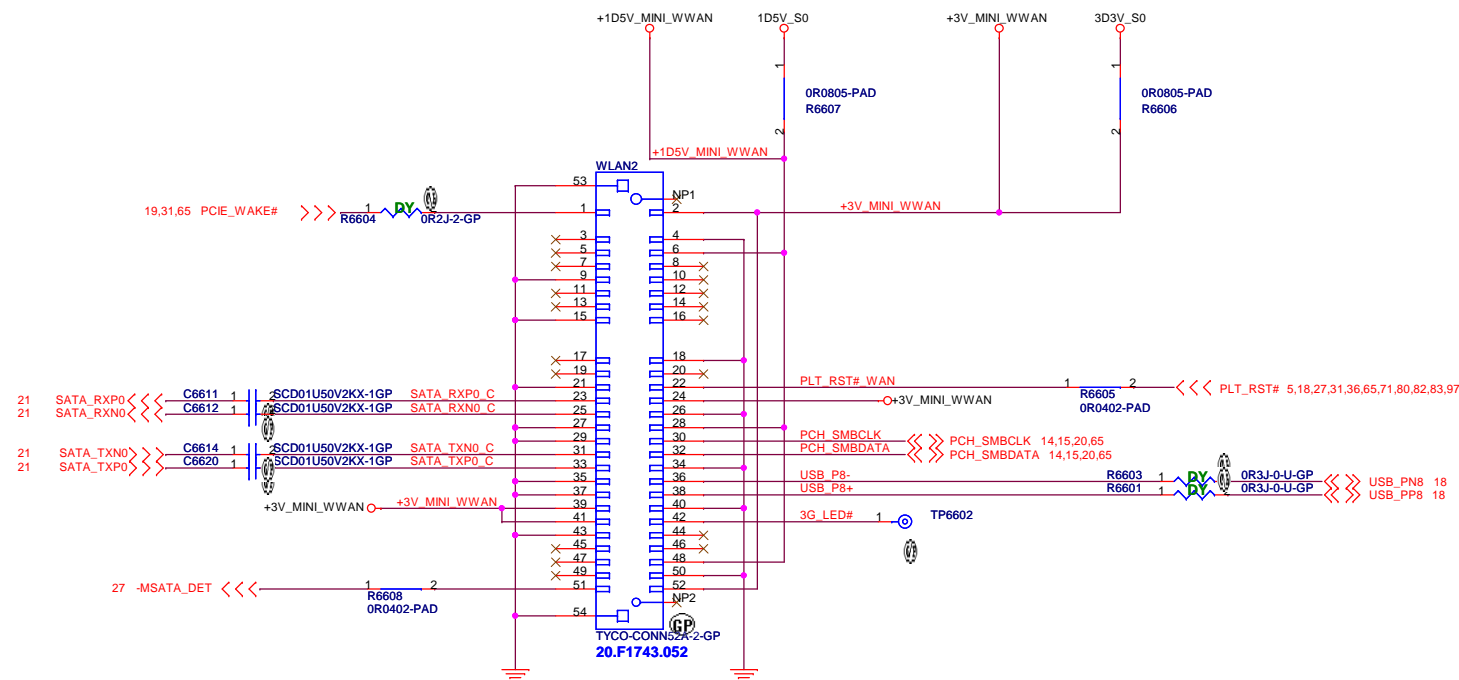
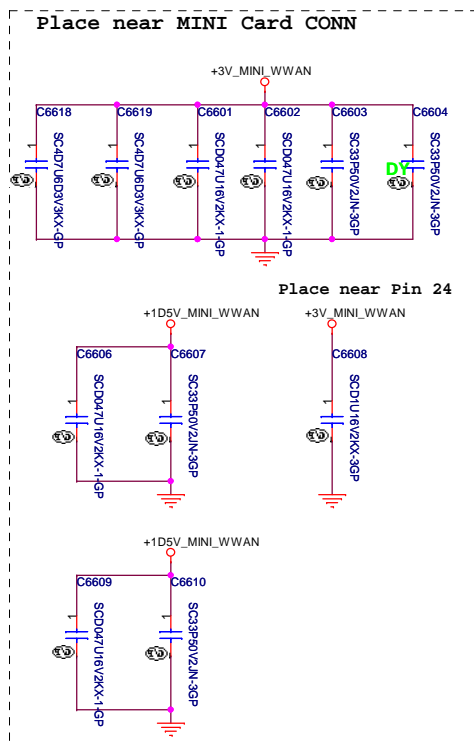
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/TP CONN
Size A3 Document Number: LA480 Rev SD
Date: Friday, January 06, 2012 Sheet 65 of 103

SSID = Wireless

mSATA for V Series Only

Mini Card Connector(Full Card)



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

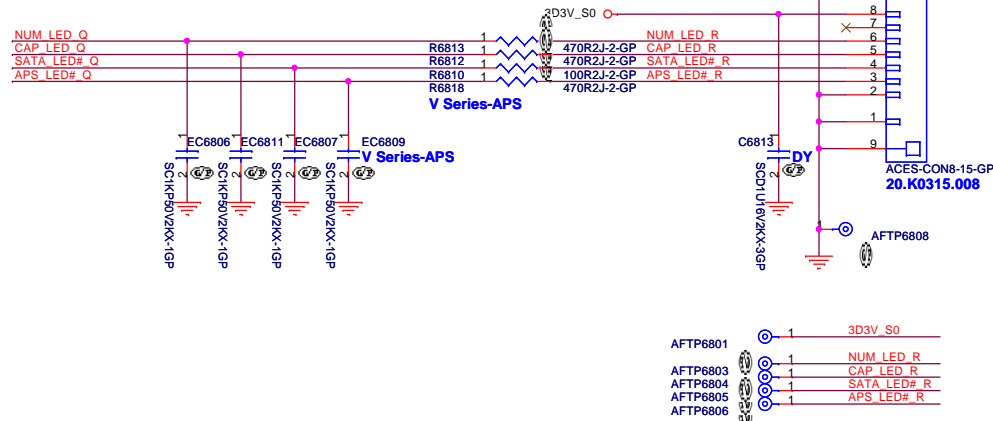
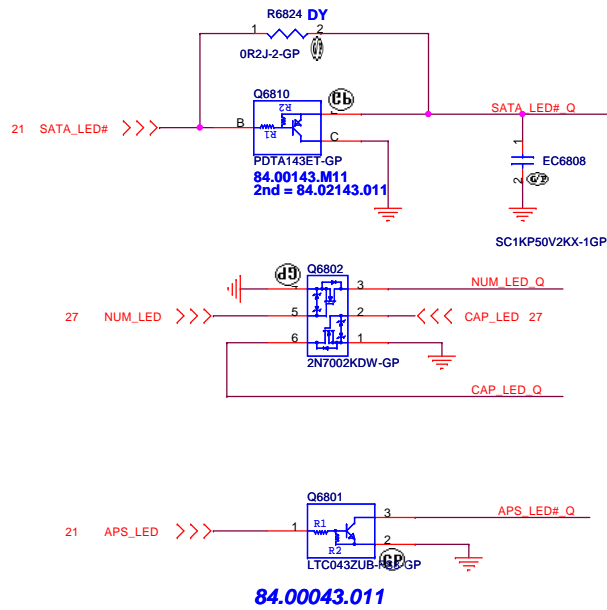
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Size	Document Number	Rev	SD
A3	LA480		
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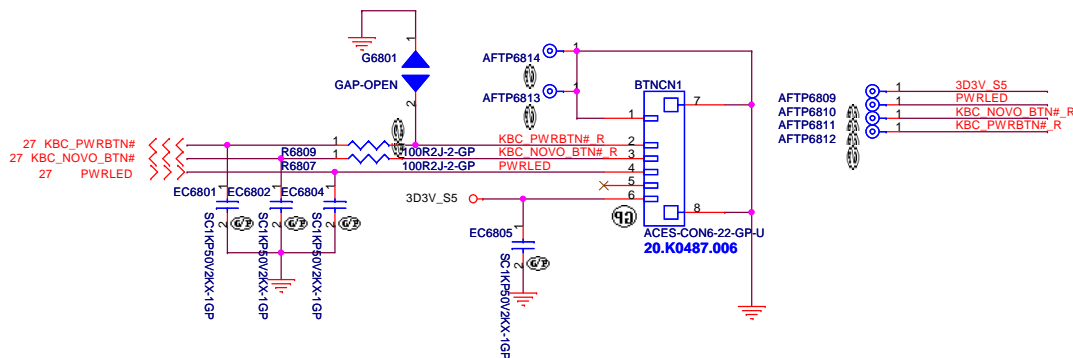
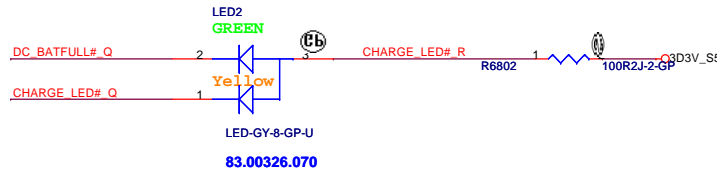
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Title Reserved			
Size A4	Document Number LA480		Rev SD
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SSID = User.Interface



CHARGER LED



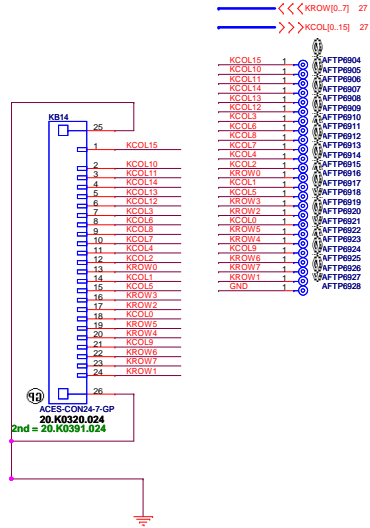
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			LED Bar/Power Button
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	68 of 103

SSID = KBC

Internal Keyboard Connector

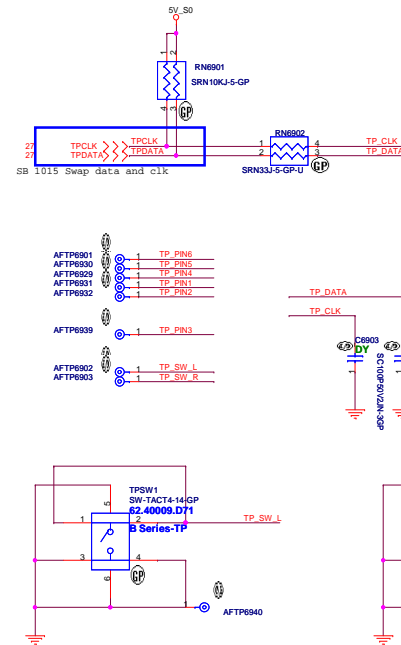


KB14 for 14" VB480 & VB485
KB15 for 15" VB580 & VB585

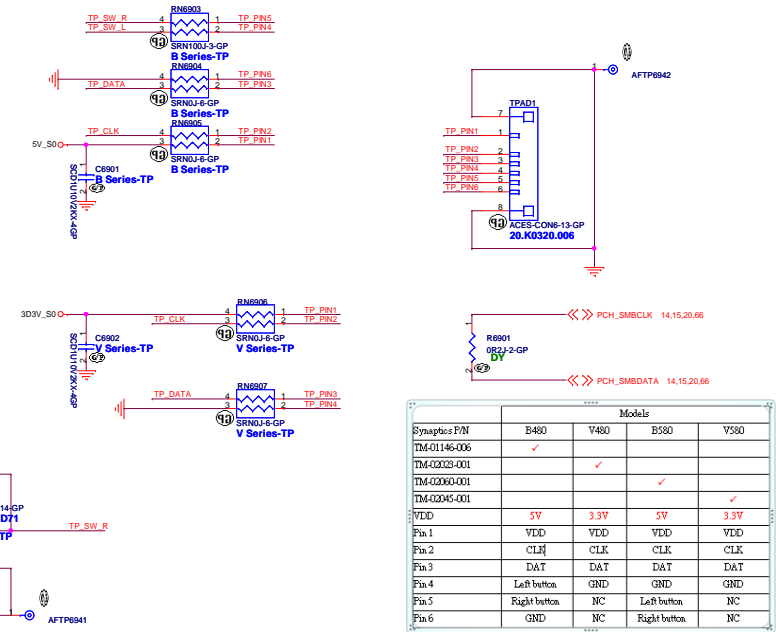
* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad

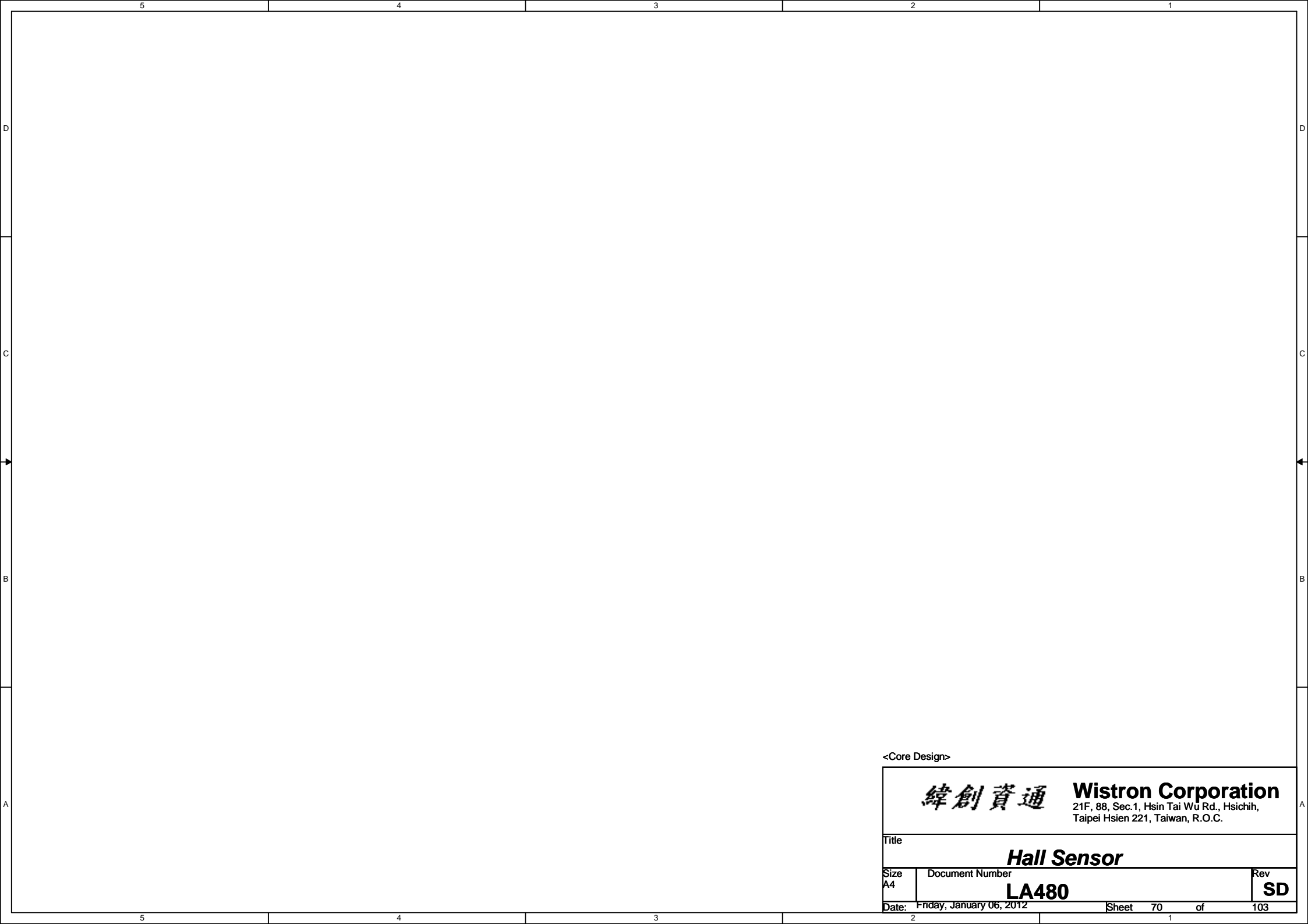


Normal Pad for B Series 5V
ClickPad for V Series 3.3V



	Models			
Synaptics P/N	B480	V480	B580	V580
TM-01146-006	✓			
TM-0202-001		✓		
TM-0206-001			✓	
TM-0204-001				✓
VDD	5V	3.3V	5V	3.3V
Fin 1	VDD	VDD	VDD	VDD
Fin 2	CLK	CLK	CLK	CLK
Fin 3	DAT	DAT	DAT	DAT
Fin 4	Left button	GND	GND	GND
Fin 5	Right button	NC	Left button	NC
Fin 6	GND	NC	Right button	NC

<Core Design>



<Core Design>

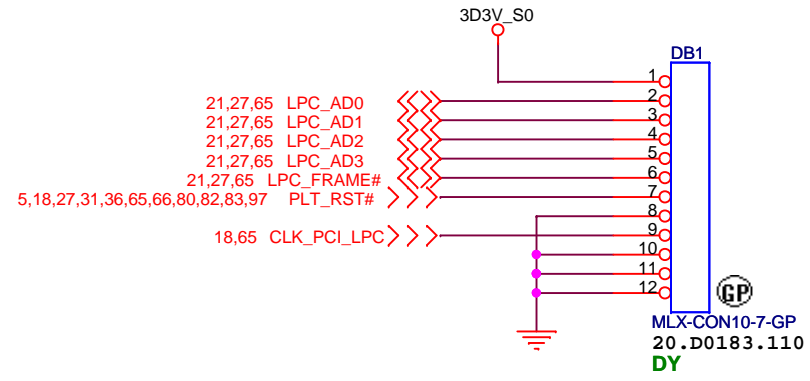
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size A4	Document Number LA480	Rev SD
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Taipei Hsien 221, Taiwan, R.O.C.

Title				
Dubug connector				
Size A4	Document Number			Rev
	LA480			SD
Date:	Friday, January 06, 2012		Sheet 71 of	103

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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 72 of	103

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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 73 of	103



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Title

CARD Reader CONN

Size
A2

Document Number
LA480

Date
Friday, January 06, 2012

Rev
SD

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

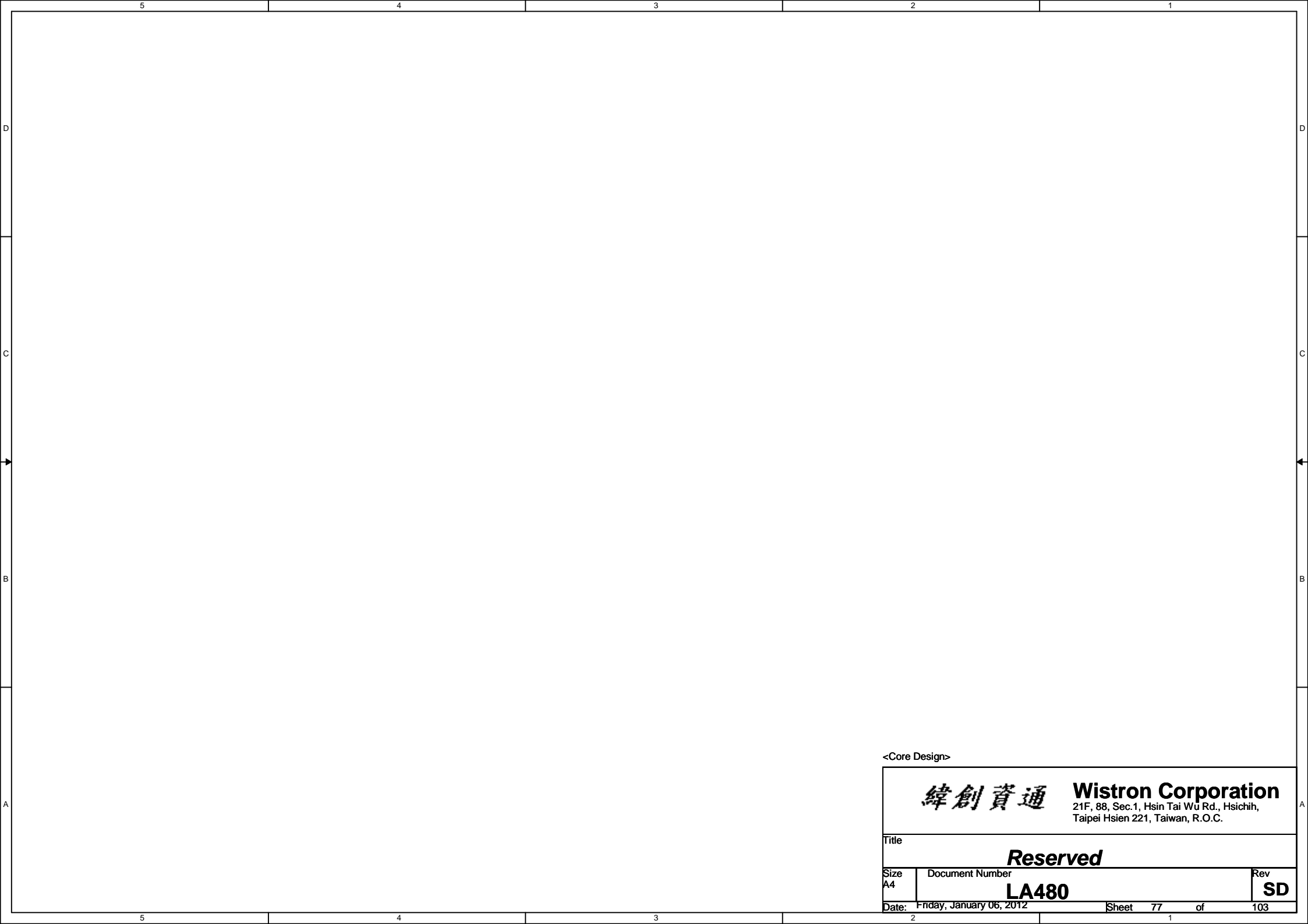
New Card

Size A4	Document Number LA480	Rev SD
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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 76 of	103



<Core Design>

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Title

Reserved

Size
A4

Document Number

LA480

Rev
SD

Date: Friday, January 06, 2012

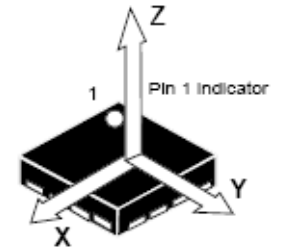
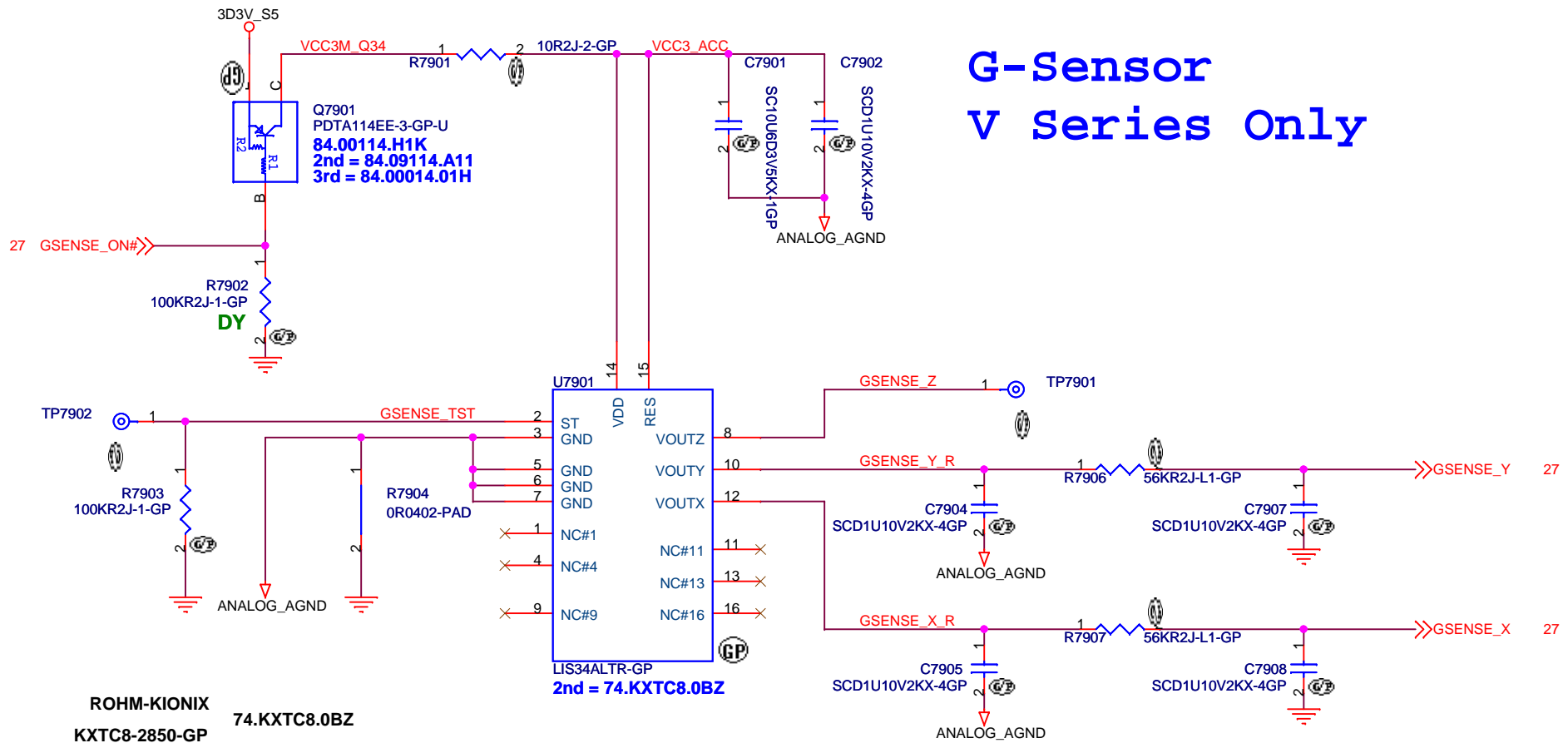
Sheet 77 of 103

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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
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G-Sensor V Series Only



Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.

<Core Design>

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Title

G-Sensor

Size
A4

Document Number

LA480

Rev
SD

Date: Friday, January 06, 2012

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RFID

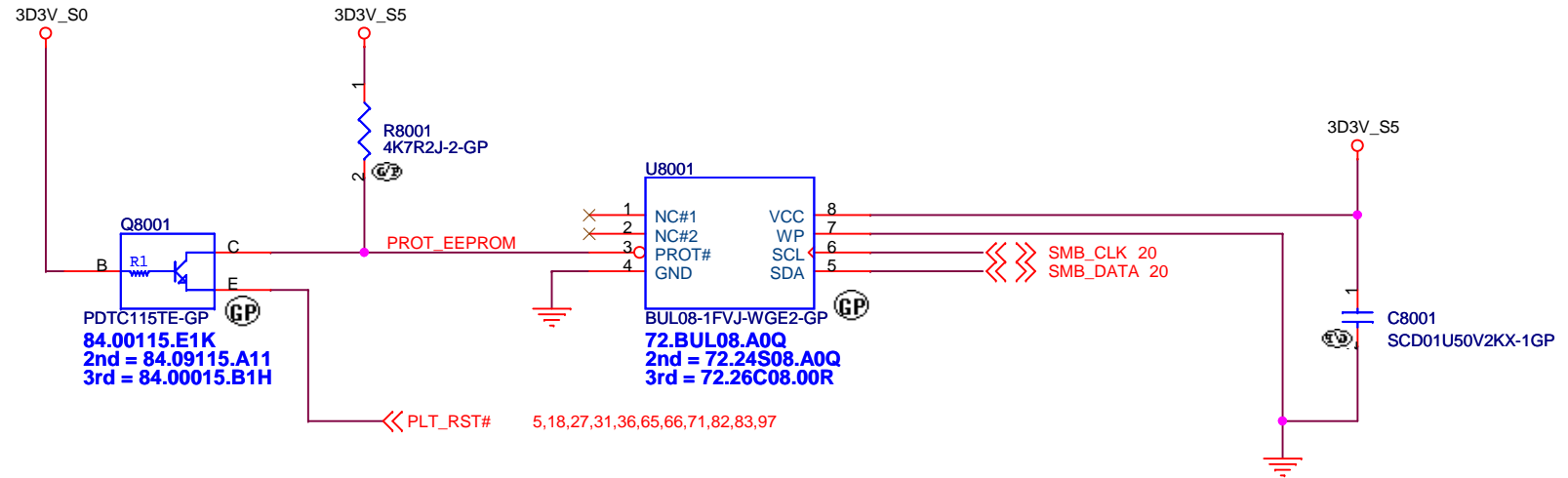


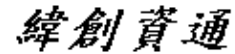
Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

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RF ID	
Size A4	Document Number LA480
Date: Friday, January 06, 2012	Rev SD
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

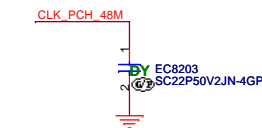
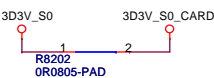
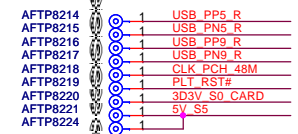
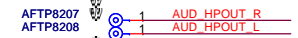
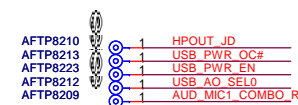
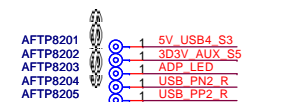
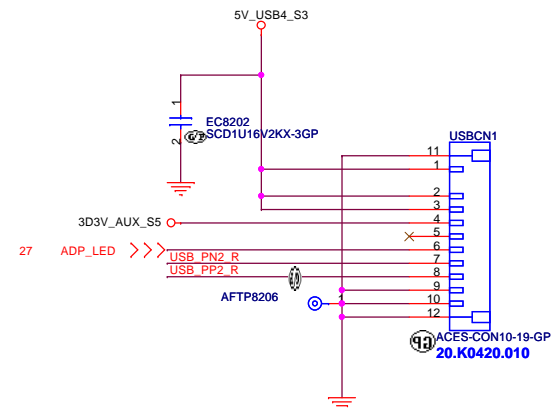
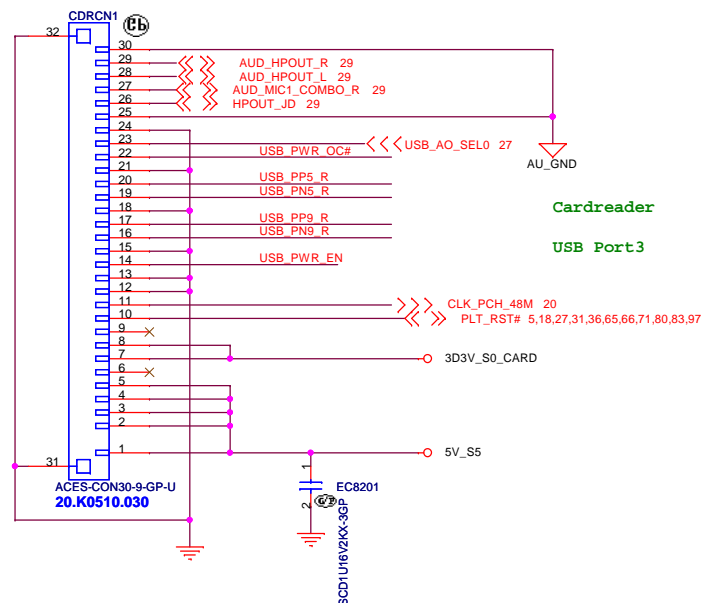
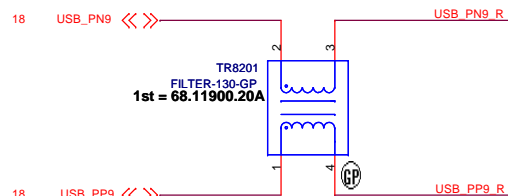
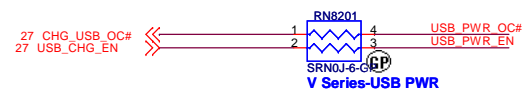
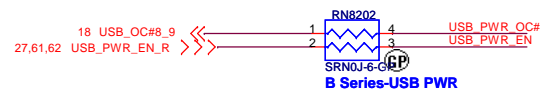
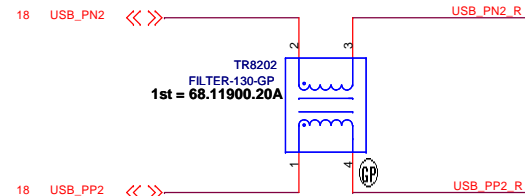
LA480

Rev
SD

Date: Friday, January 06, 2012

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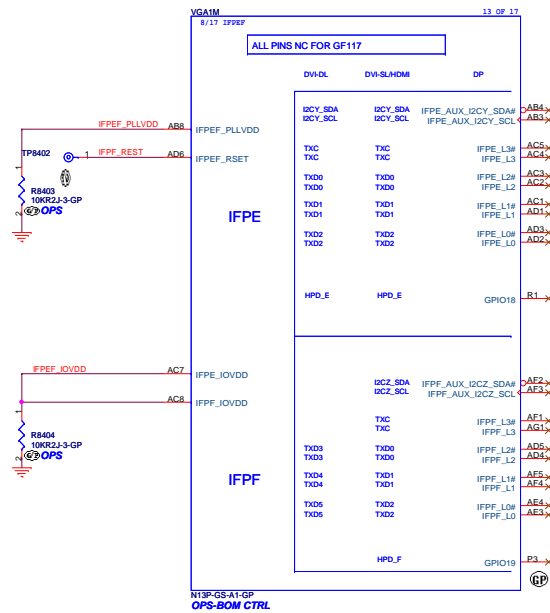
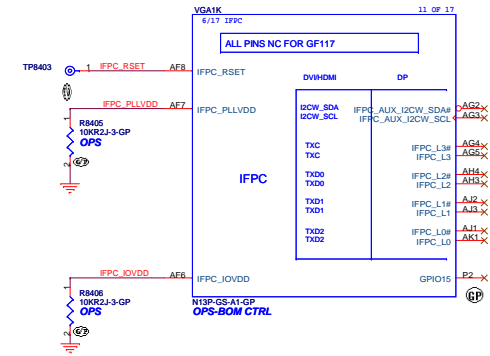
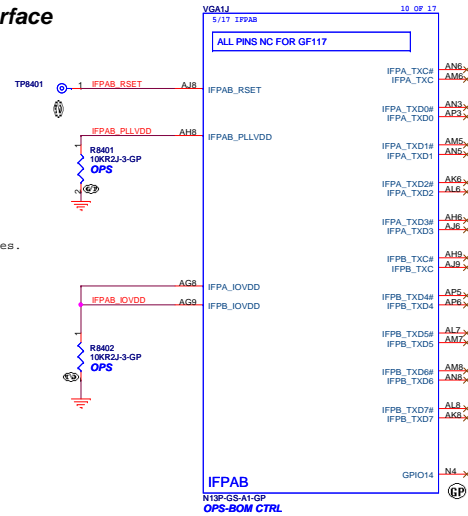
R8201 and R8203 Dual layout with TR8201



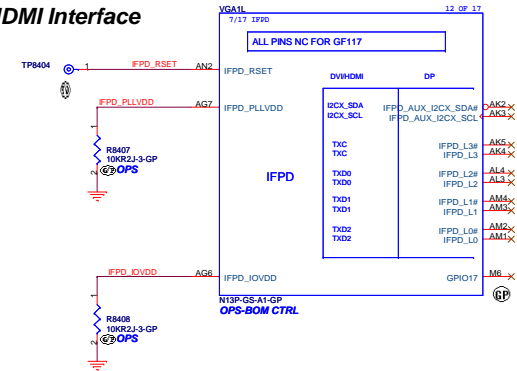


LVDS Interface

SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.



HDMI Interface

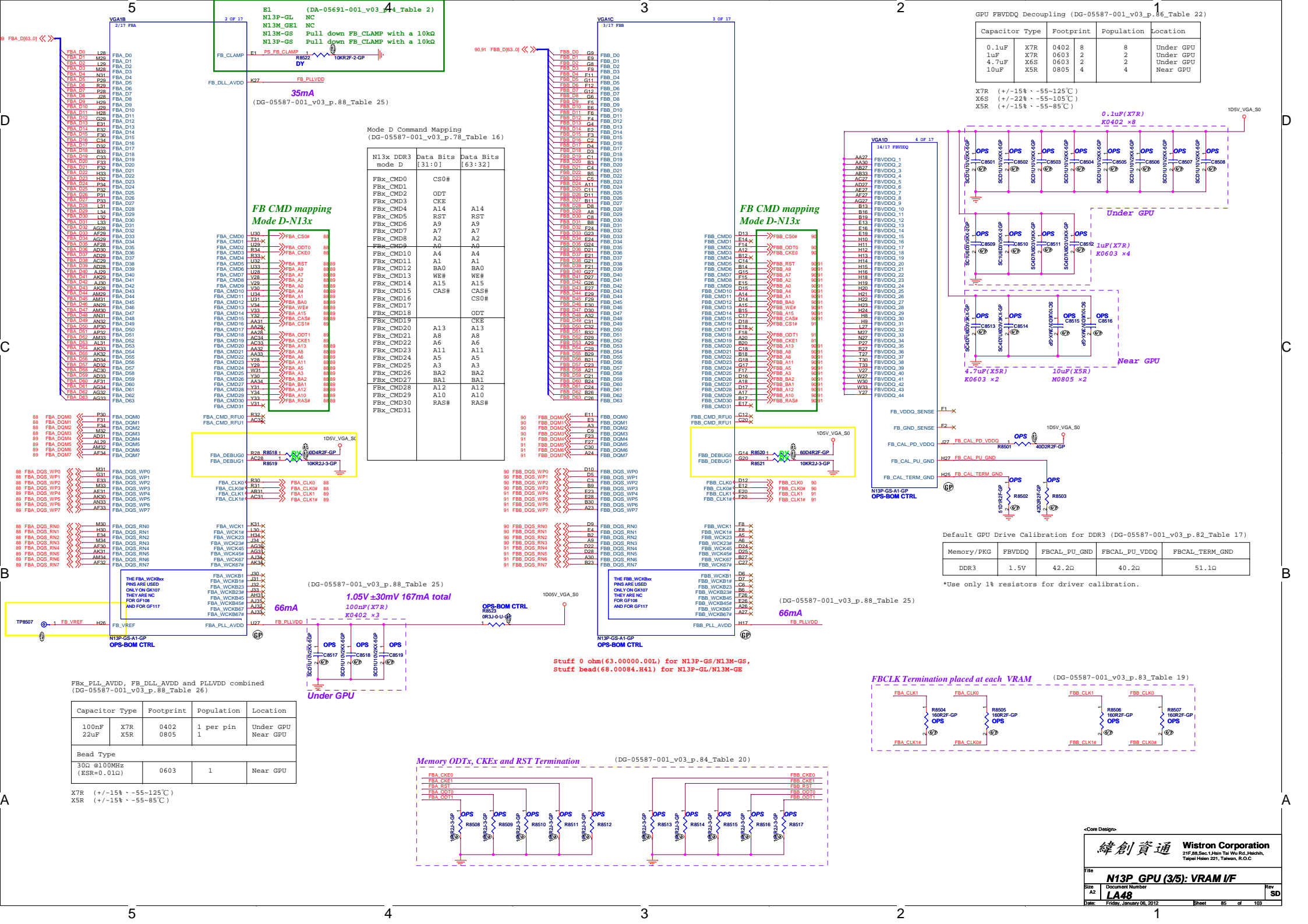


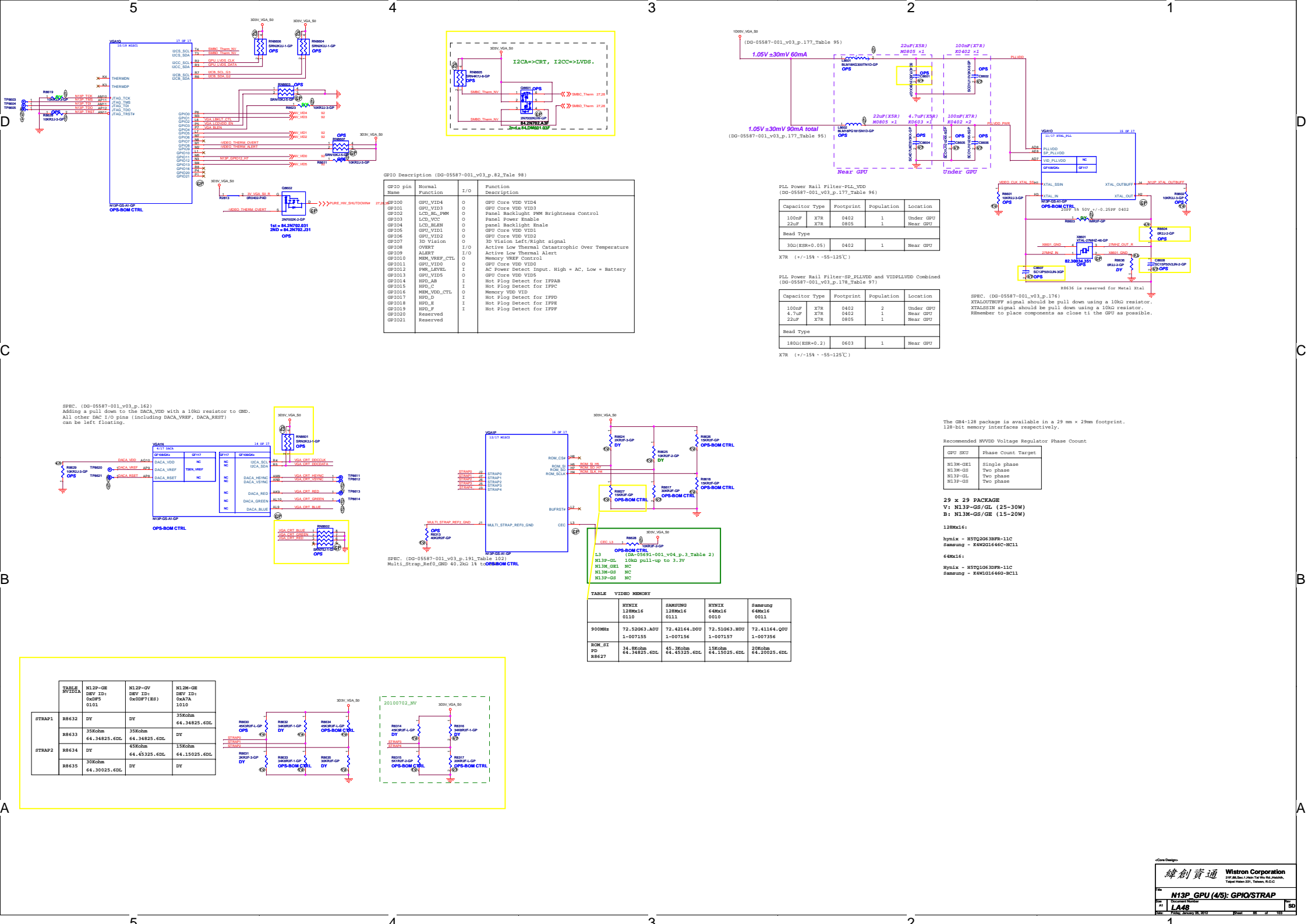
<Core Design>

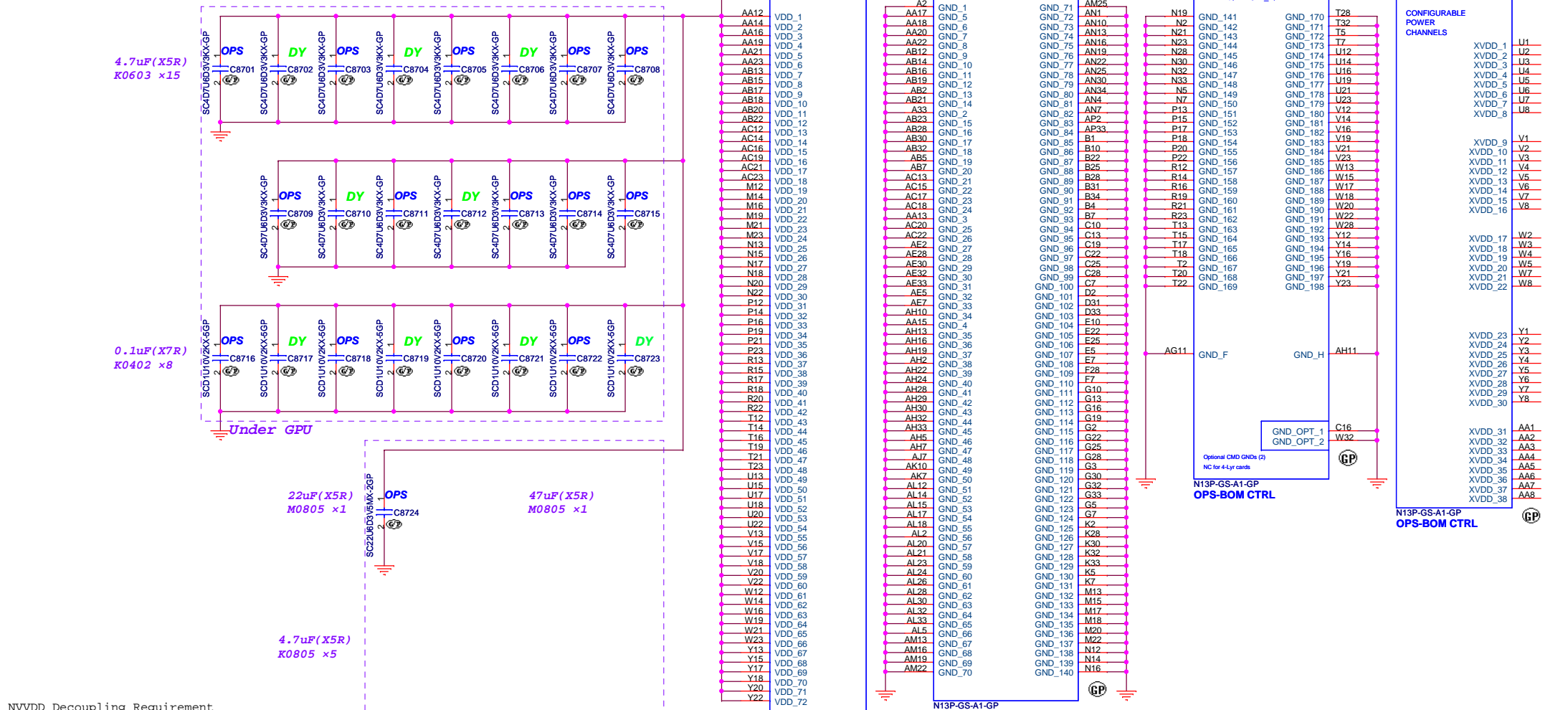
緯創資通 Wistron Corporation
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Taipei Hsin 221, Taiwan, R.O.C.

Title **N13P_GPU (2/5): DIGITALOUT**

Size A2	Document Number LA48	Rev SD
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NVVDD Decoupling Requirement
(DG-05587-001_v03_p.56_Table 7)

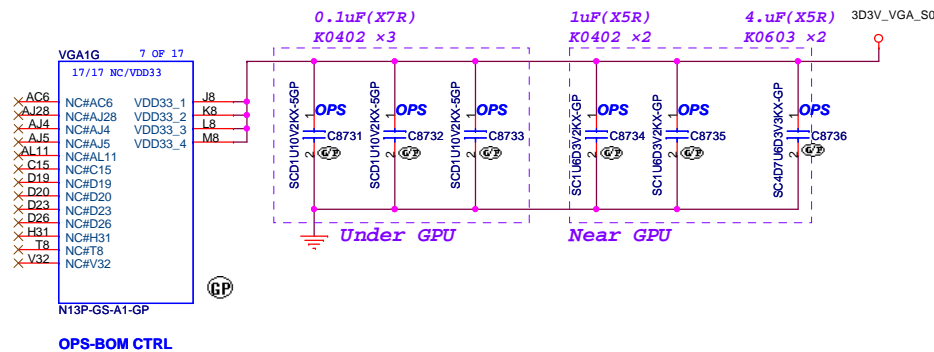
Capacitor Type	Footprint	Population	Location
4.7uF	X6S	0603	15
0.1uF	X7R	0402	8
47uF	X5R	0805	1
22uF	X5R	0805	1
4.7uF	X5R	0805	5

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

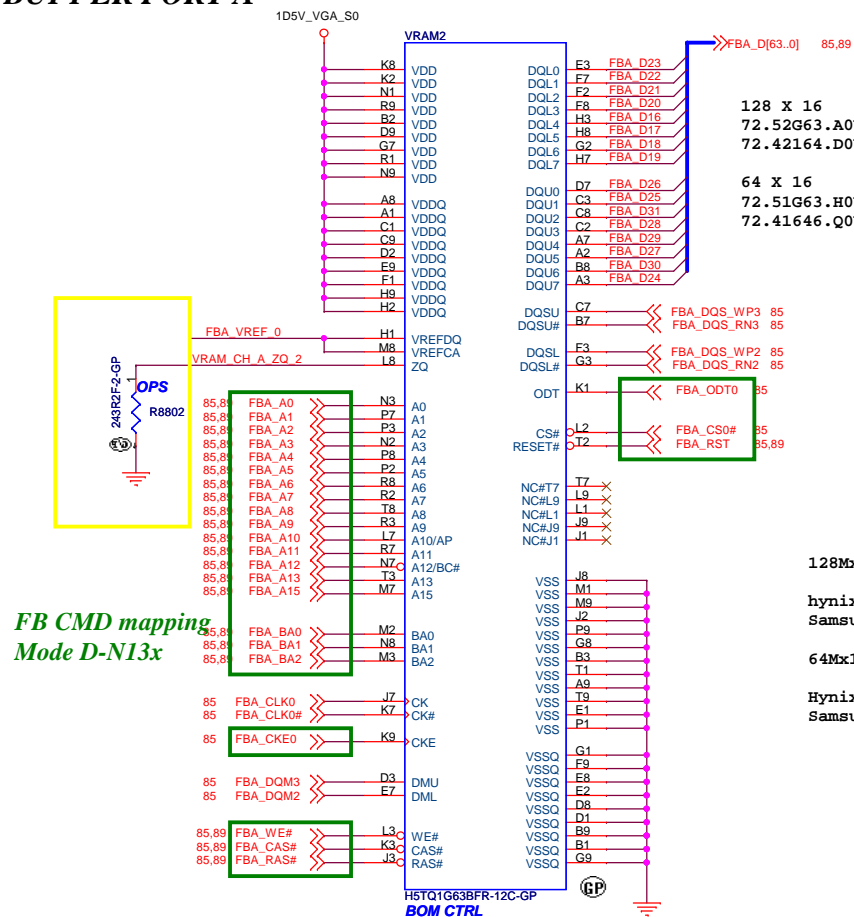
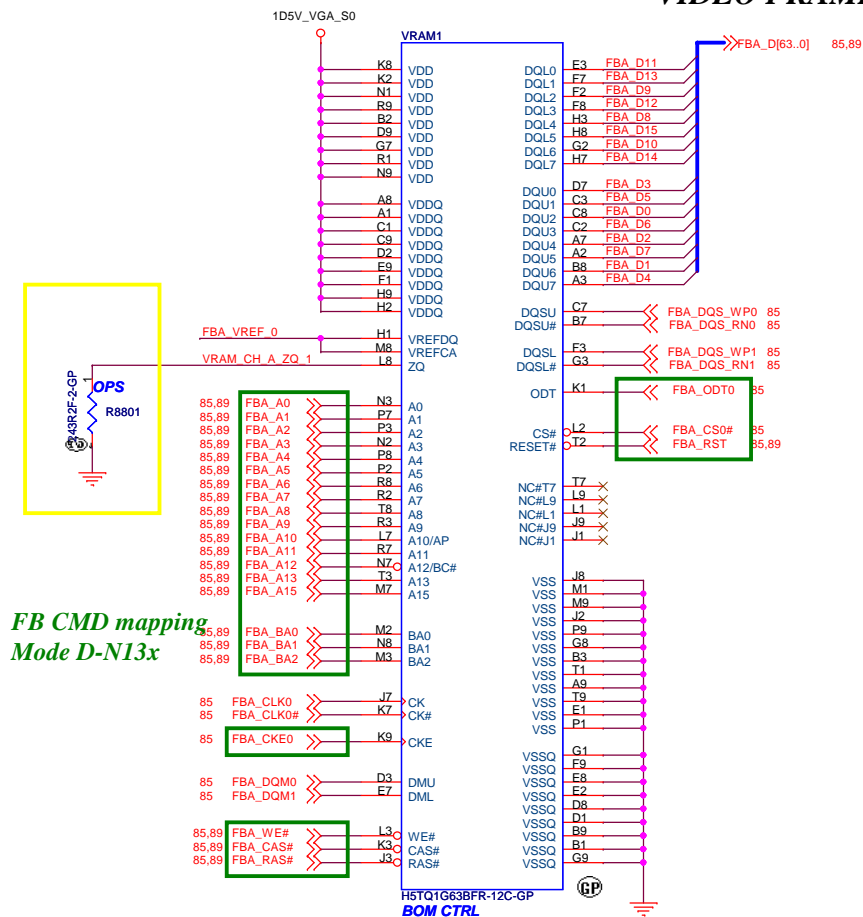
Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	3
1uF	X5R	0402	2
4.7uF	X5R	0603	1

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)



<Core Design>

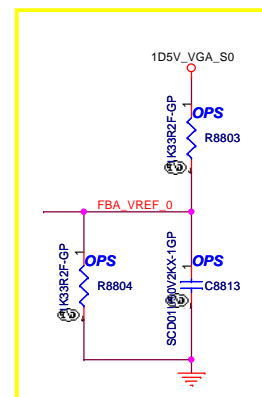
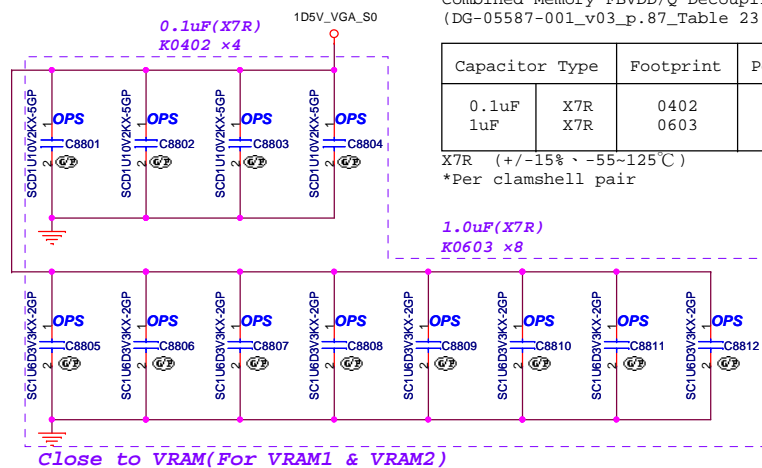
VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125°C)
*Per clamshell pair



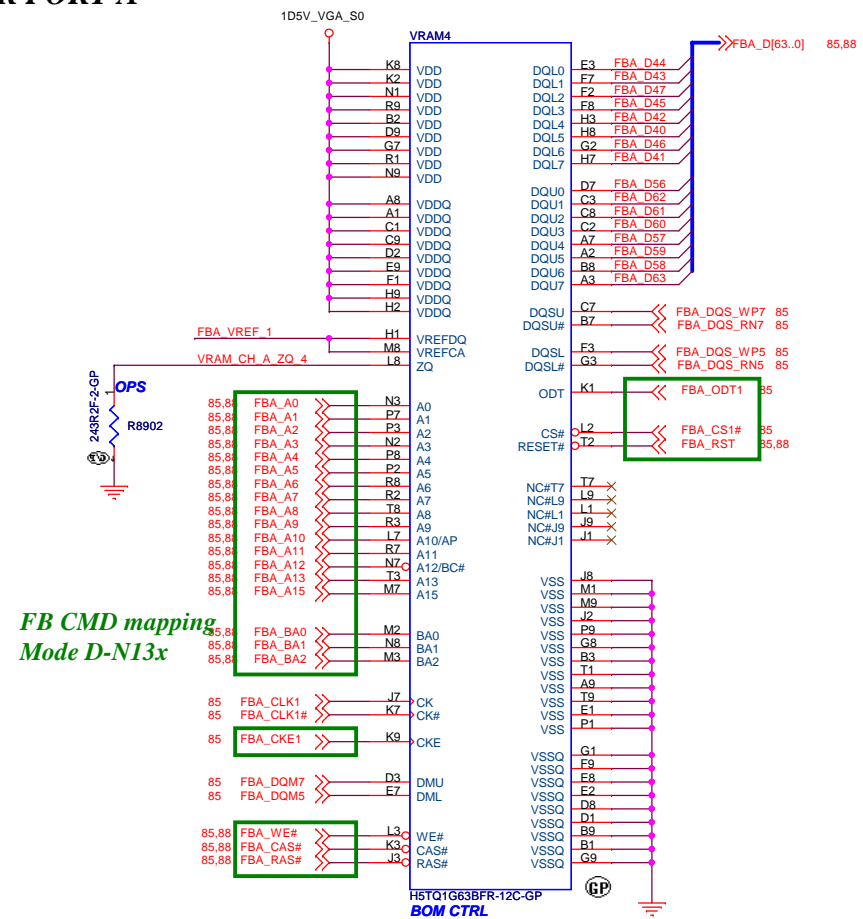
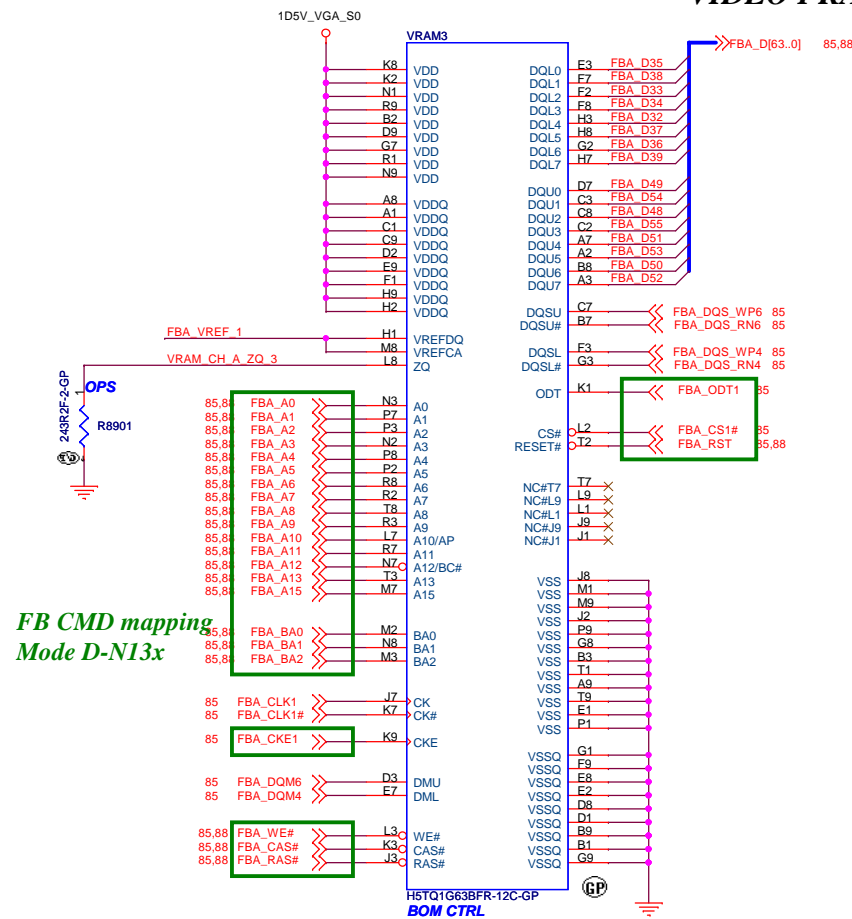
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Title	CHANNEL-A_VRAM1,2 (1/4)
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Size A3	Document Number LA48	Rev SD
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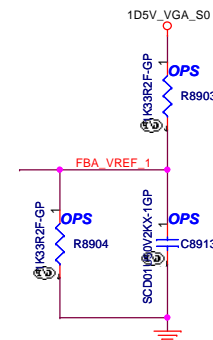
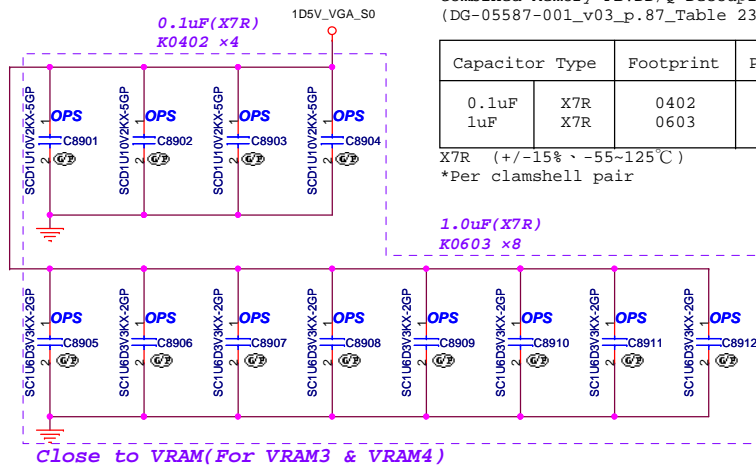
VIDEO FRAME BUFFER PORT A



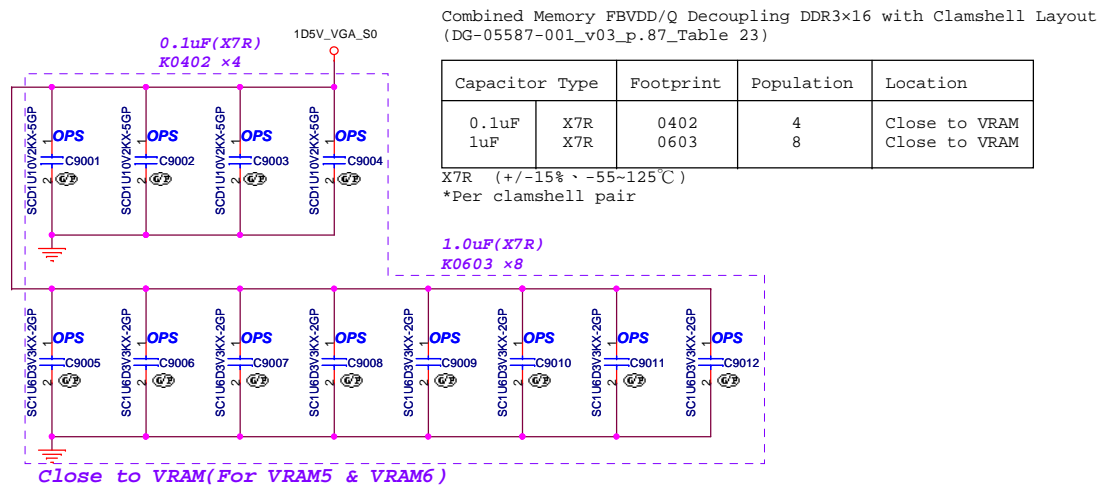
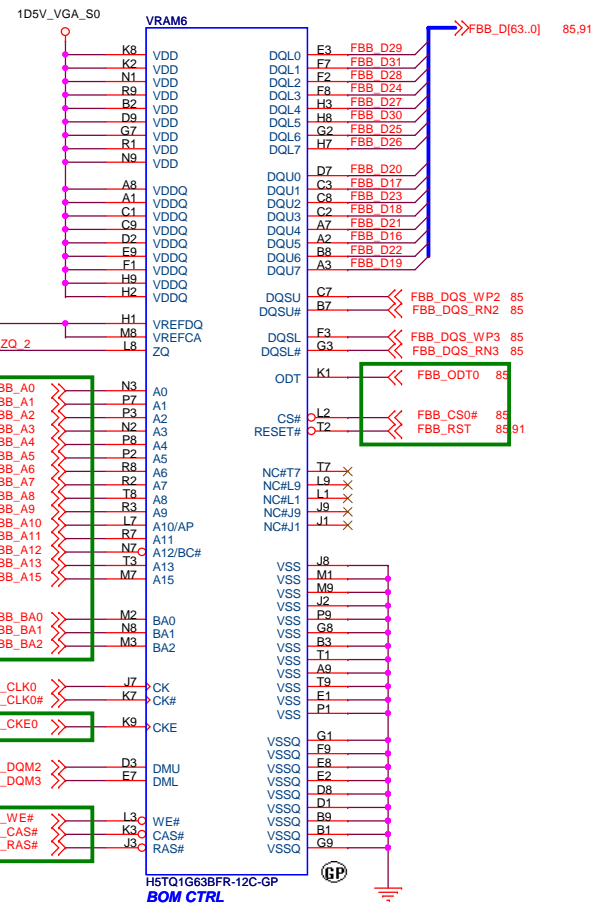
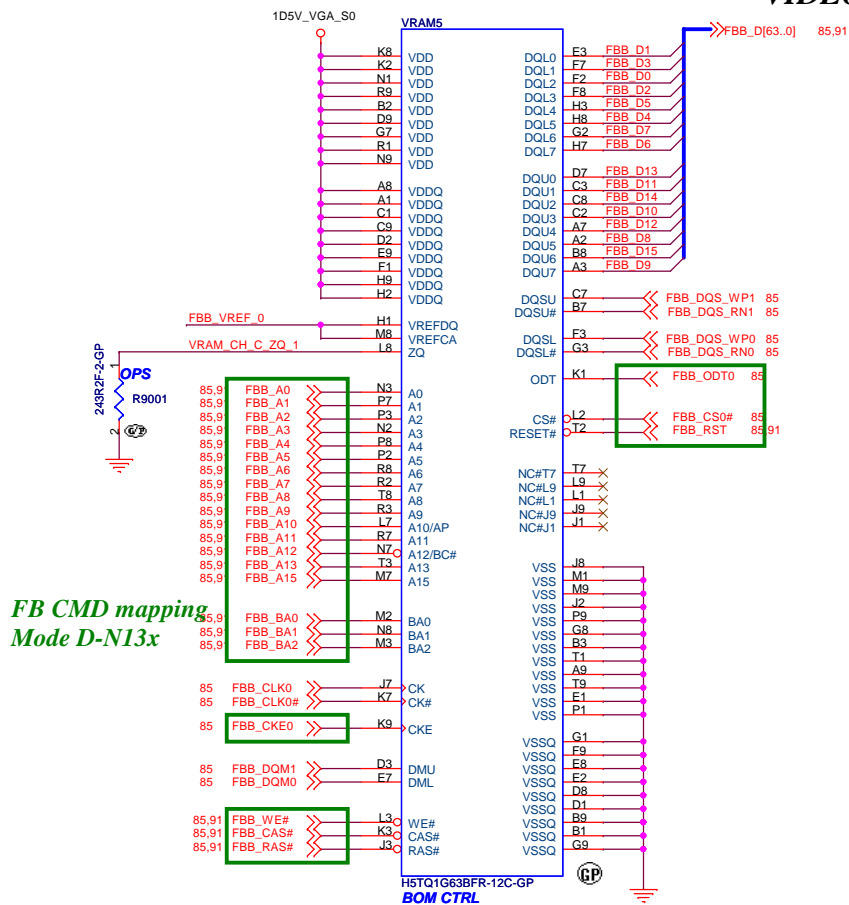
Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125°C)
*Per clamshell pair



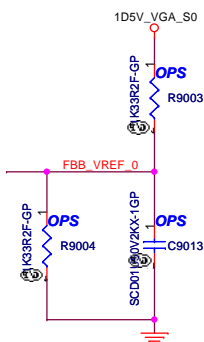
VIDEO FRAME BUFFER PORT C



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	Close to VRAM
1uF	X7R	0603	Close to VRAM

X7R (+/-15%、-55-125℃)
*Per clamshell pair



<Core Design>

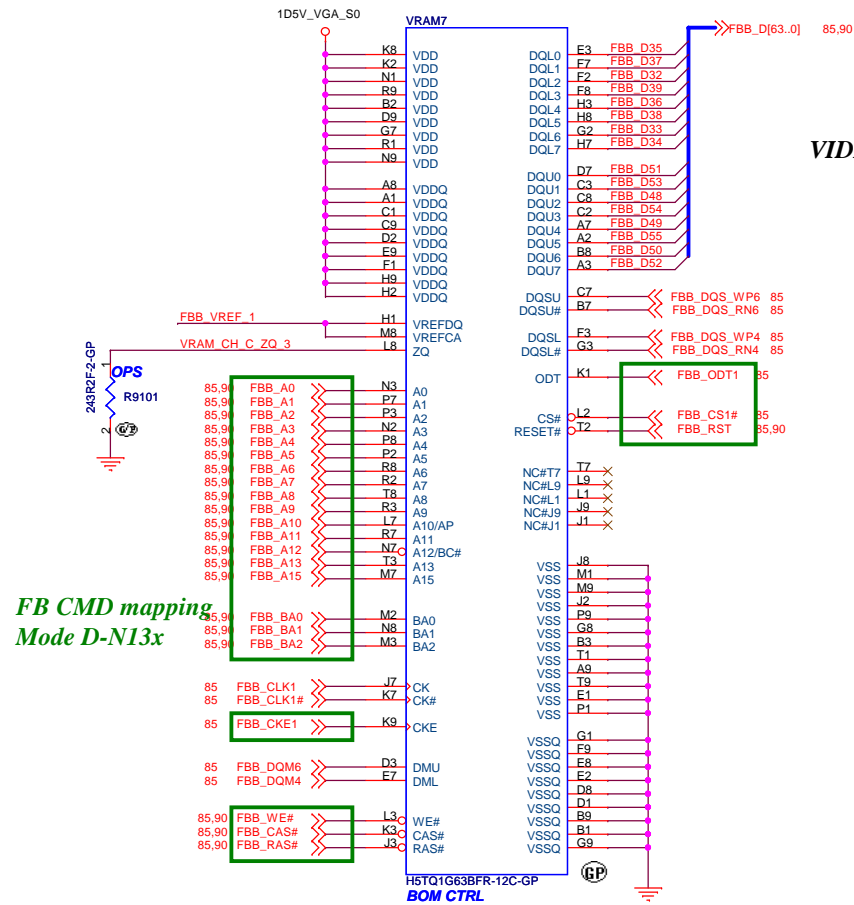
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Taipei Hsien 221, Taiwan, R.O.C.

Title **CHANNEL-C_VRAM5,6 (3/4)**

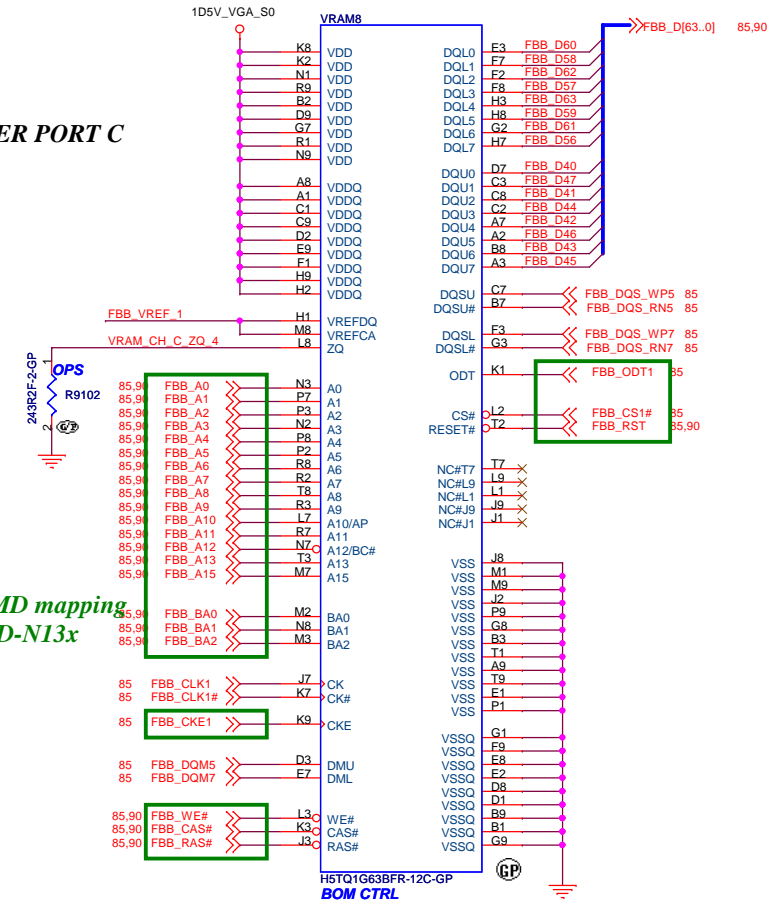
Size A3 Document Number **LA48** Rev **SD**

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VIDEO FRAME BUFFER PORT C



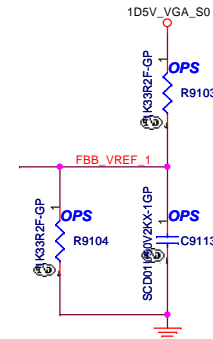
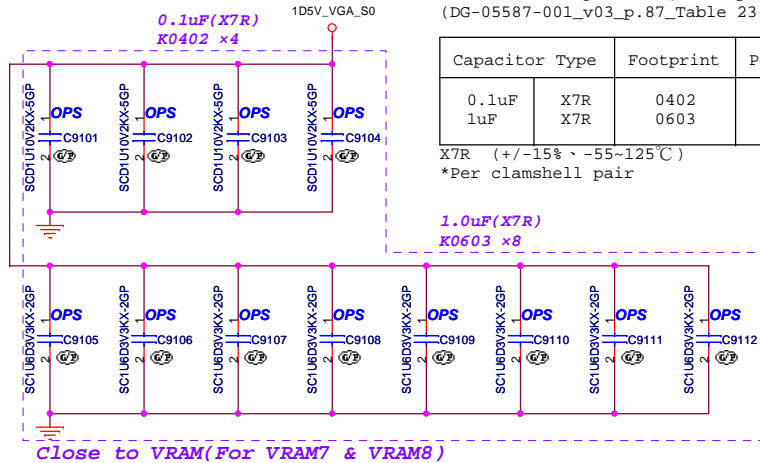
FB CMD mapping Mode D-N13x



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair



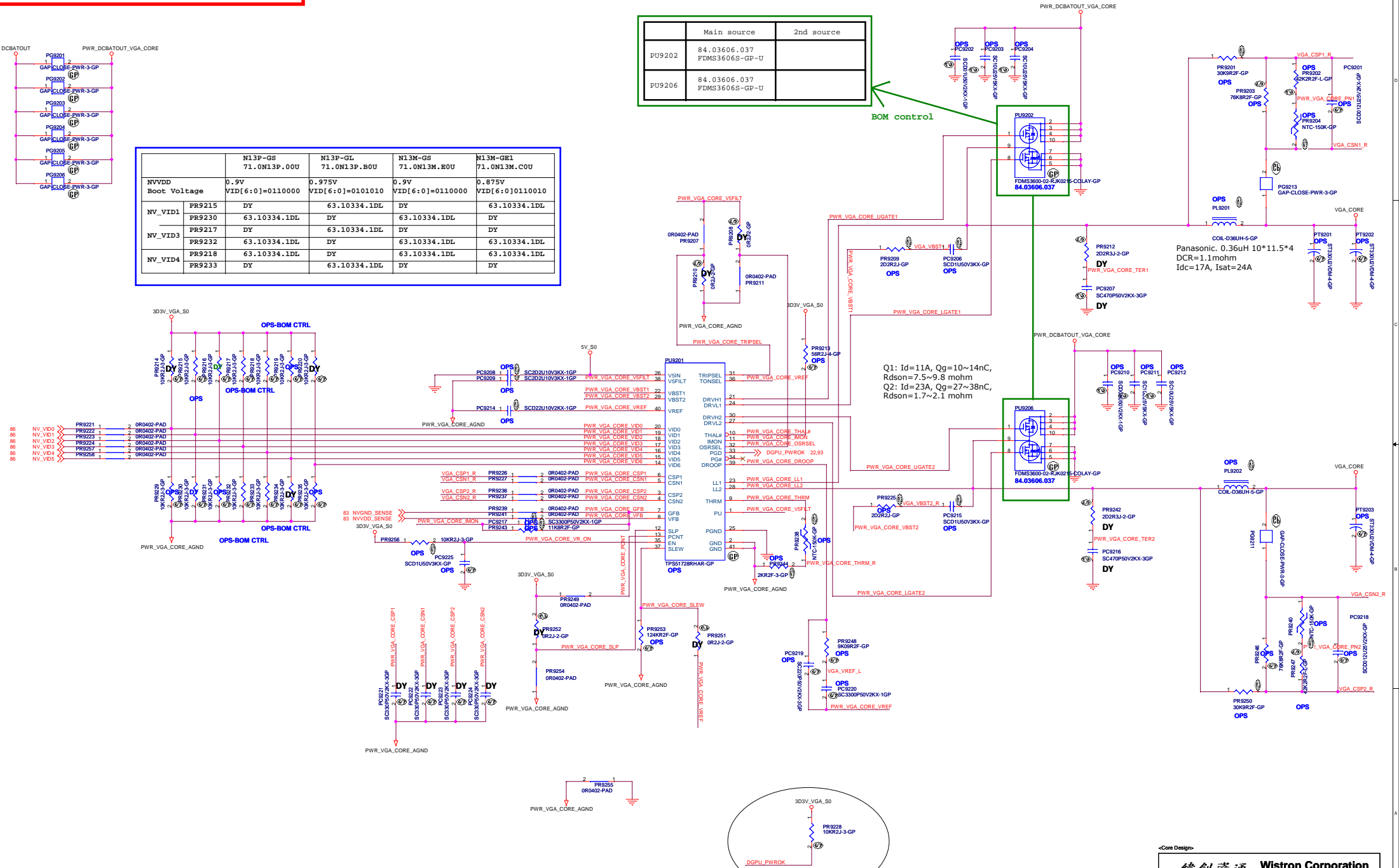
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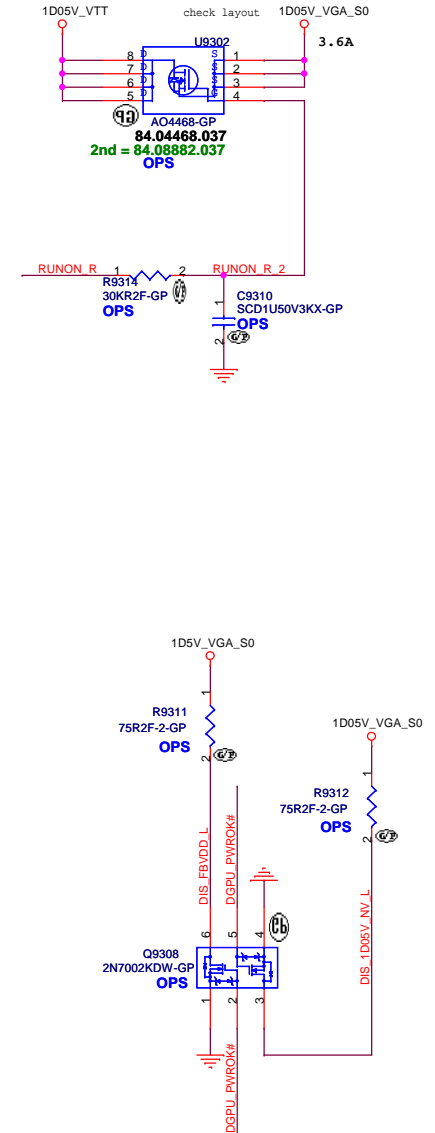
Title **CHANNEL-C_VRAM7,8 (4/4)**

Size A3 Document Number **LA48** Rev SD
Date: Friday, January 06, 2012 Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX



1.05V to 1.05V_VGA_S0 Transfer



Date: Friday, January 06, 2012 Sheet 93 of 103

D

C

B

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<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</div></div>		
Title <Title>		
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 94	of 103

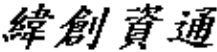
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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 95 of	103

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title TOUCH PANEL			
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CPU Plate

H14 HOLET157B276R134-GP ZZ.SCREW.091	H15 HOLET157B276R134-GP ZZ.SCREW.091	H16 HOLET157B276R134-GP ZZ.SCREW.091	H17 HOLET157B276R134-GP ZZ.SCREW.091
--	--	--	--

VGA Std-Off

H1
STF237R128H42-1-GSTF237R128H42-1-GP

H2
STF237R128H42-1-GSTF237R128H42-1-GP

H21
STF237R128H42-1-GSTF237R128H42-1-GP

34.4GD01.001 34.4GD01.001 34.4GD01.001

The schematic diagram illustrates the MINI PCIE interface. It shows a series of capacitors (SCD1J25V2XK-GP) connected to ground. The components are labeled as follows:

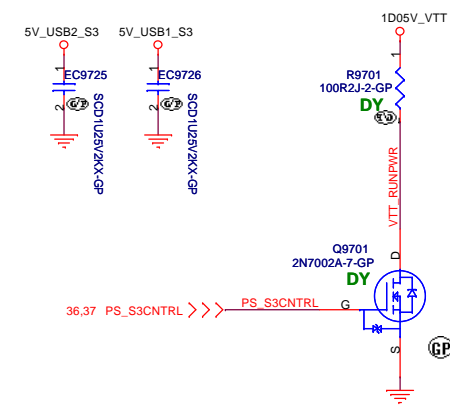
- 1GP**: A label for the first capacitor.
- H18**: A label for the first capacitor.
- STF256R89H178-GP**: A label for the first capacitor.
- 34.4B417.001**: A label for the first capacitor.
- DCBATOUT**: A label for the first capacitor.
- VCCSA**: A label for the first capacitor.
- EC9729**, **EC9727**, **EC9728**, **EC9730**, **EC9731**, **EC9732**, **EC9733**: Labels for the capacitors connected to the SCD1J25V2XK-GP capacitors.
- SCD1J25V2XK-GP**: The capacitor value for all capacitors.

```

-->>> XDP_DBRESET# 5,19
-->>> H_CPUPIWRGD 5,22
-->>> PLT_RST# 5,18,27,31,36,65,66,71,80,82,83

```

14" Structure boss



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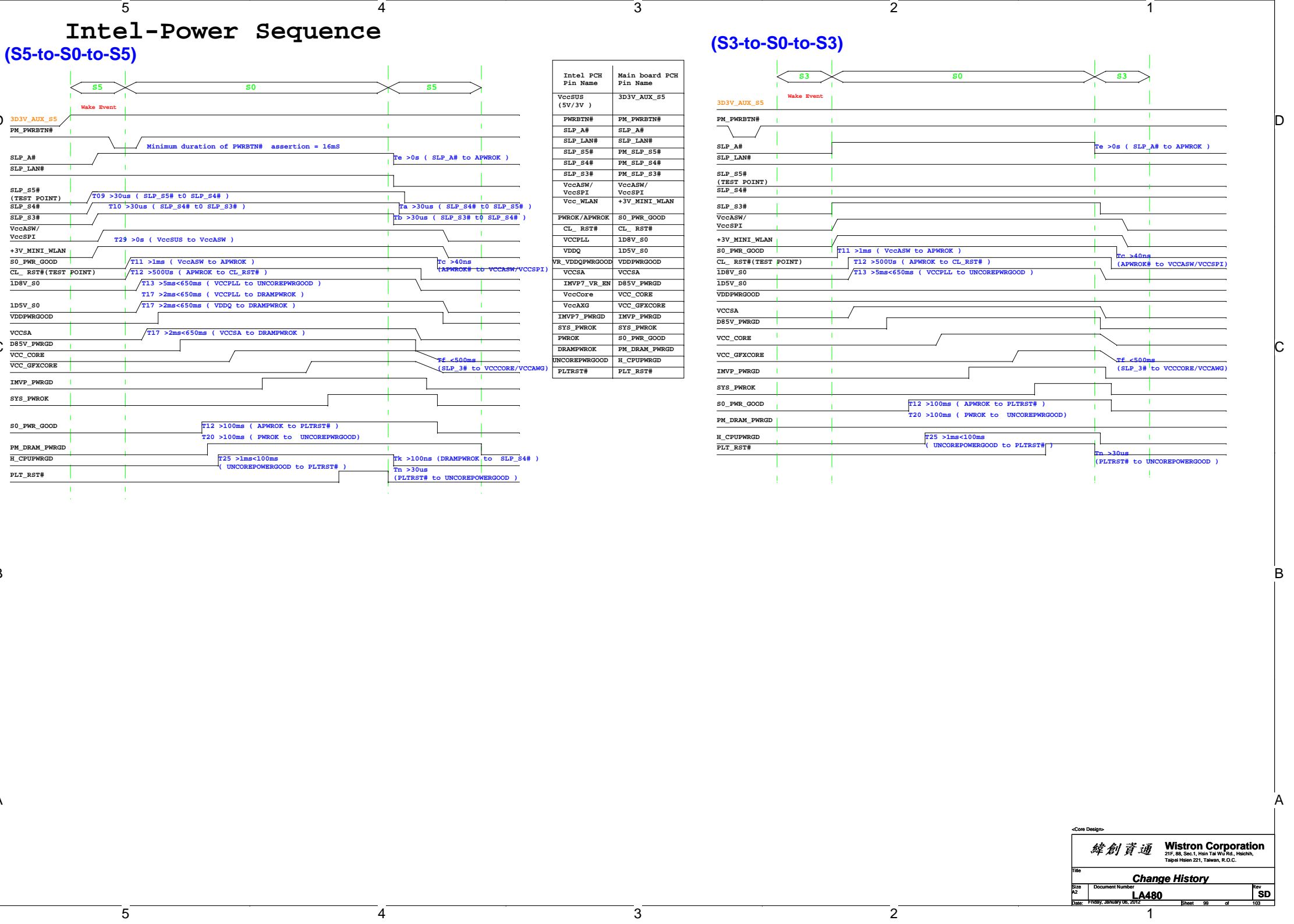
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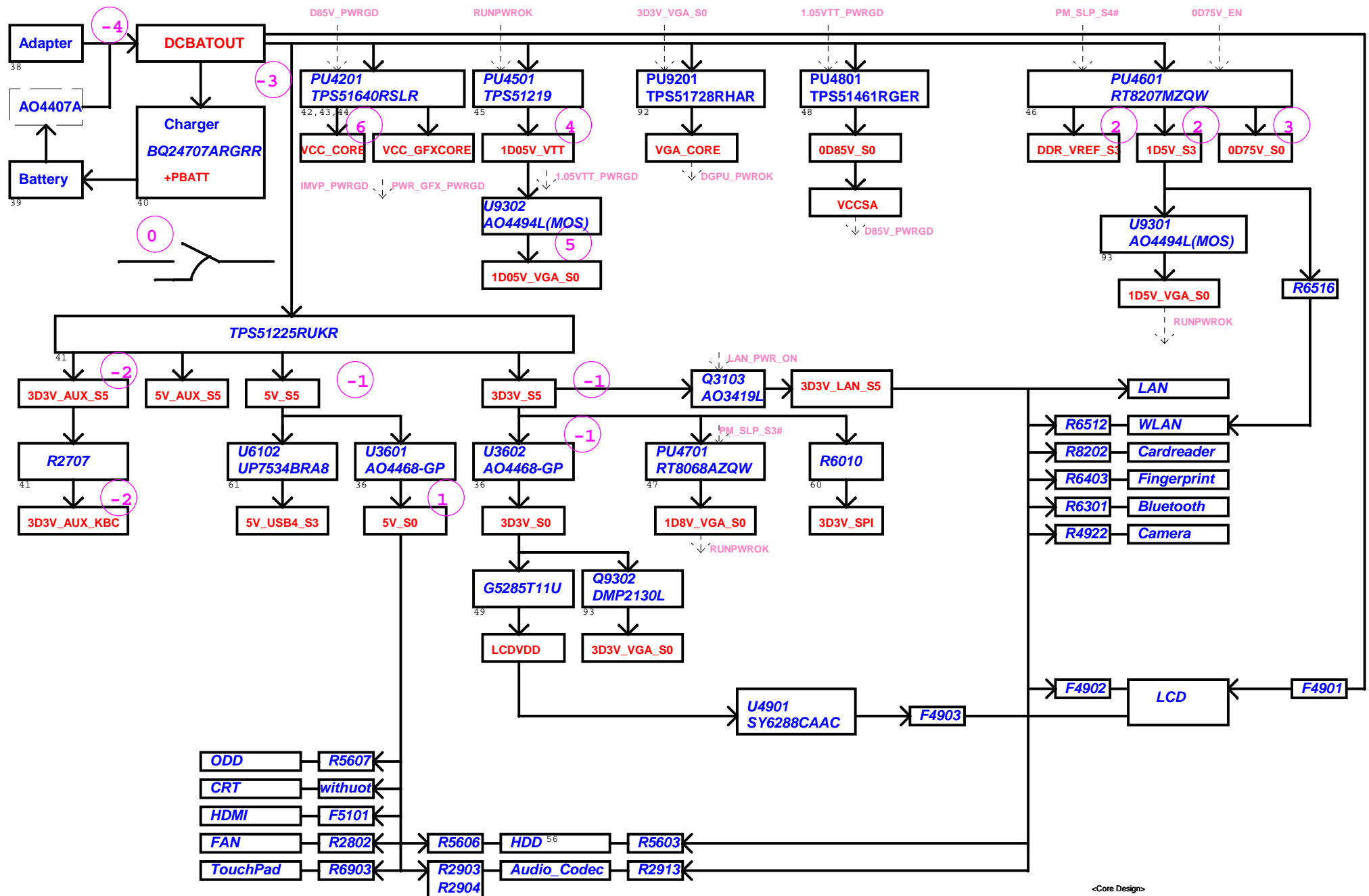
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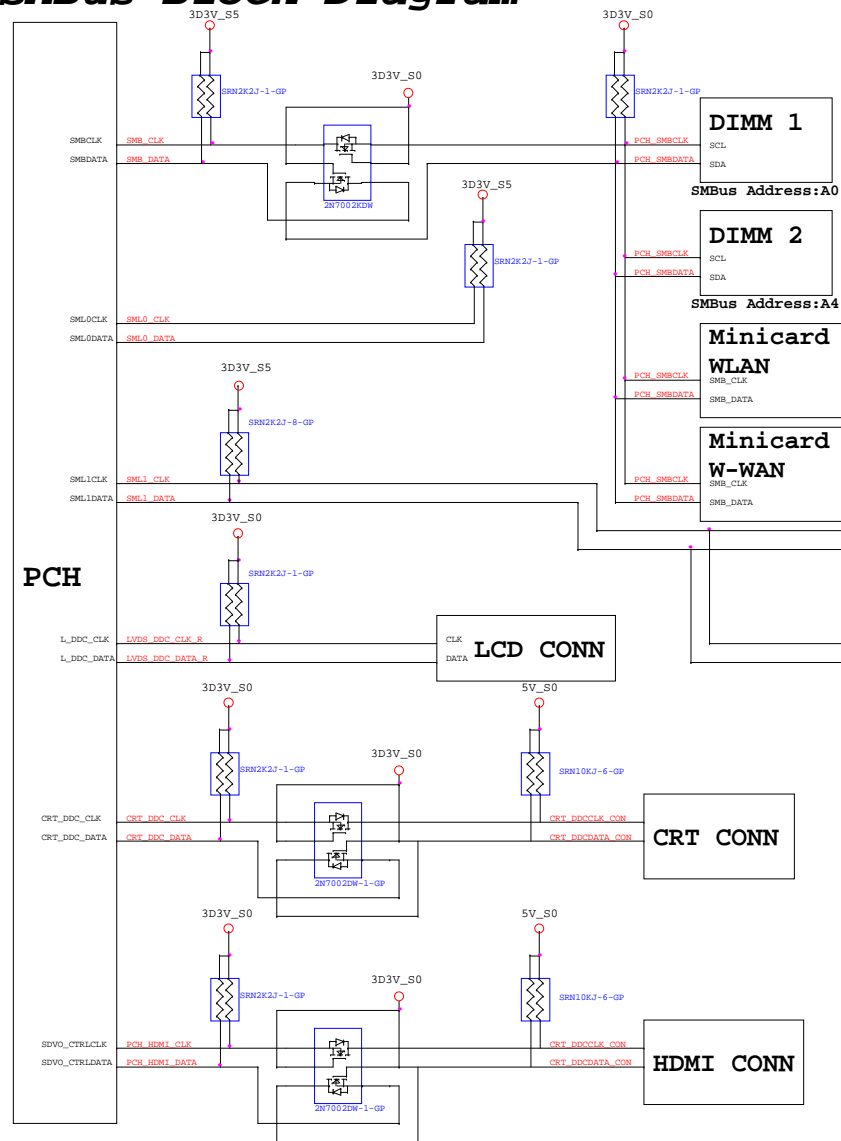
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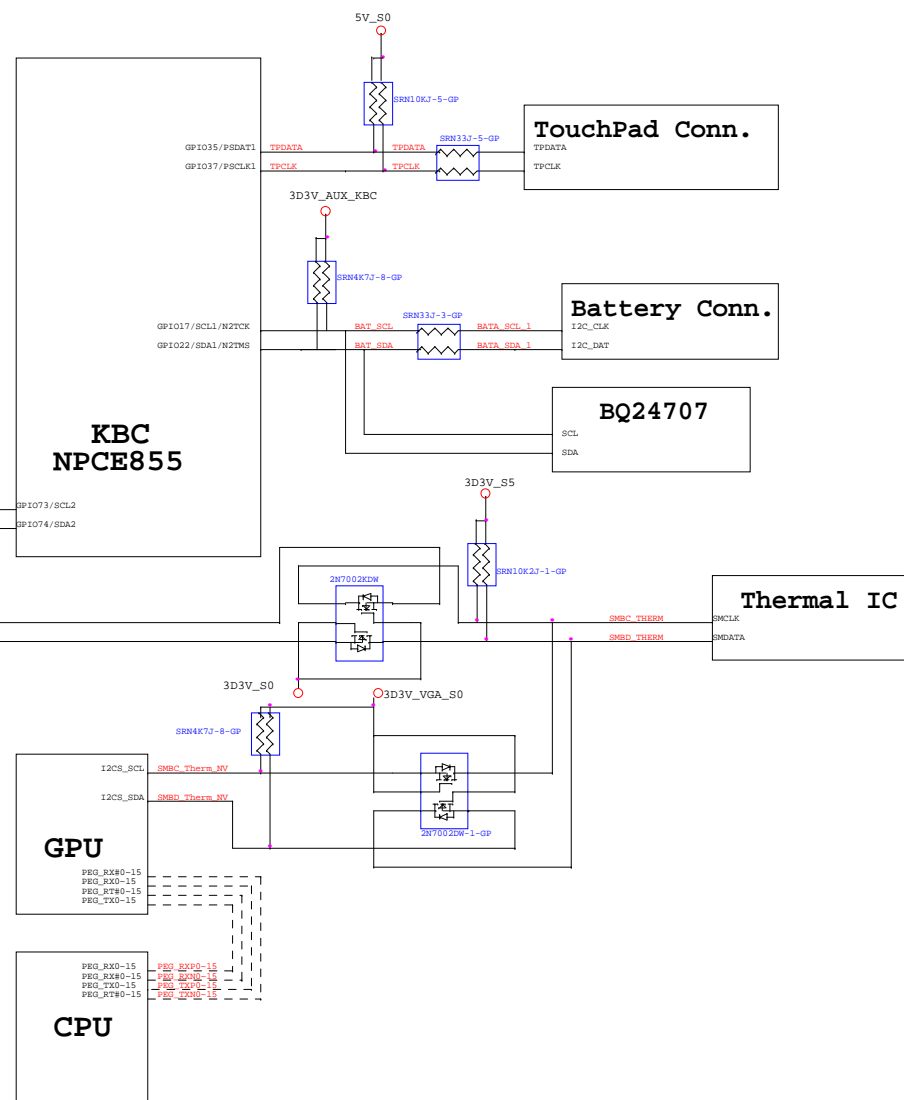
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Title		
Power Block Diagram		
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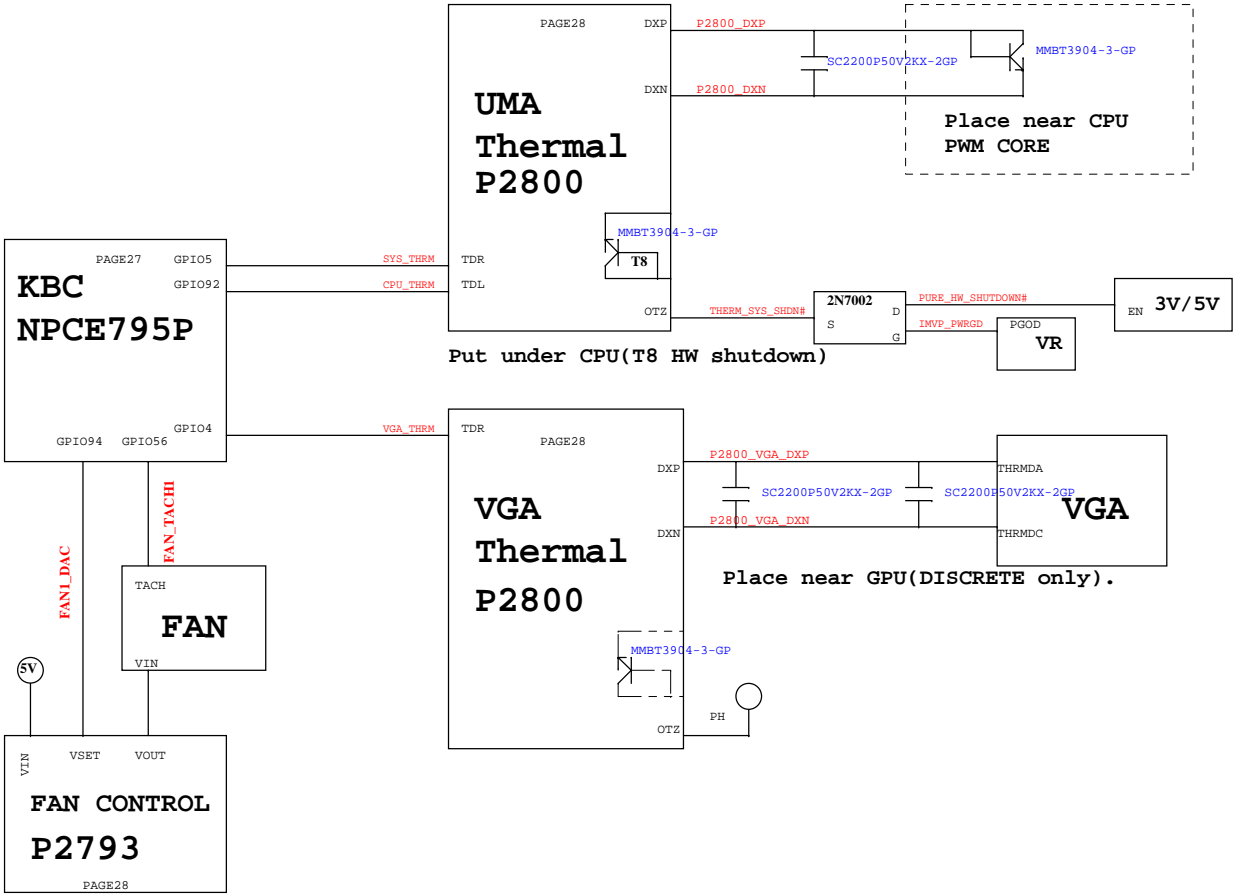
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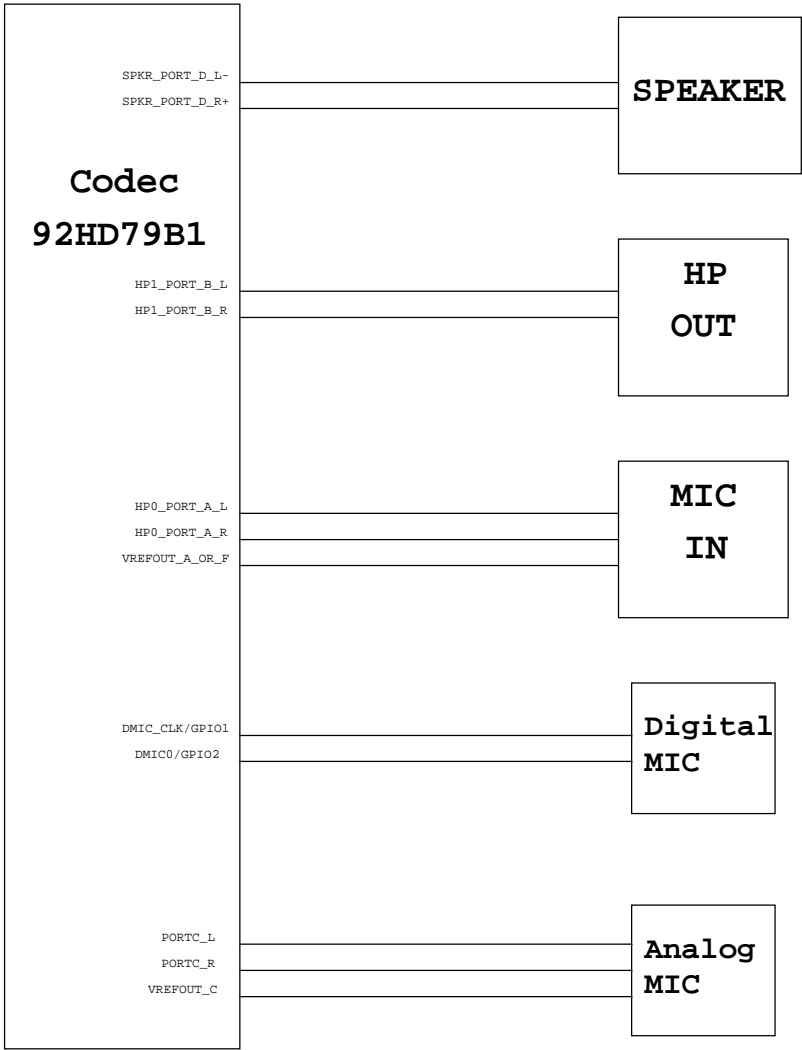
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



5	4	3	2	1
D				
C				
B				
A				

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<i>Change History</i>			
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